Circuit diagram of ZTEX USB-FPGA-Module 1.15y (rev. 2)

Contents:

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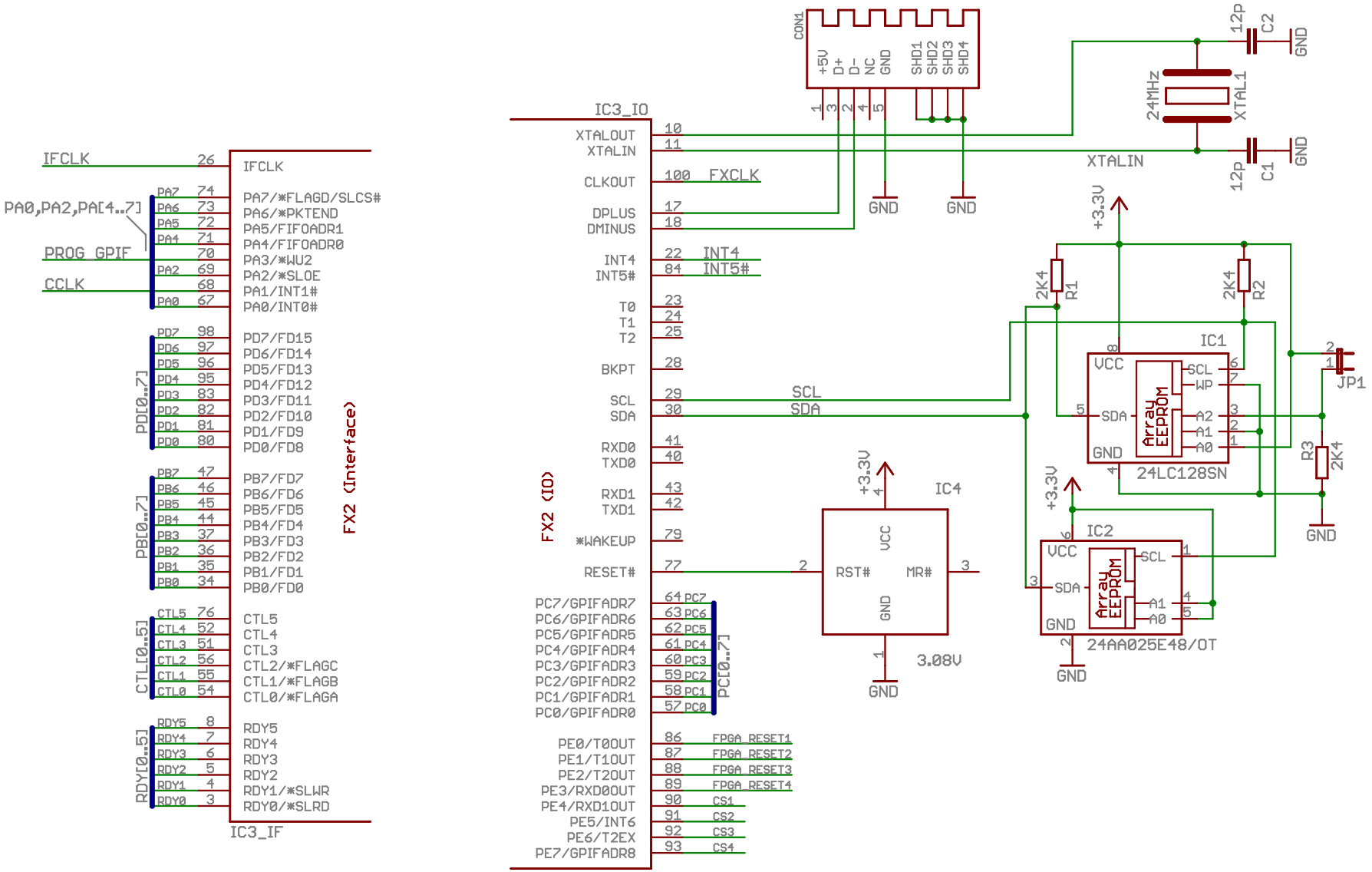
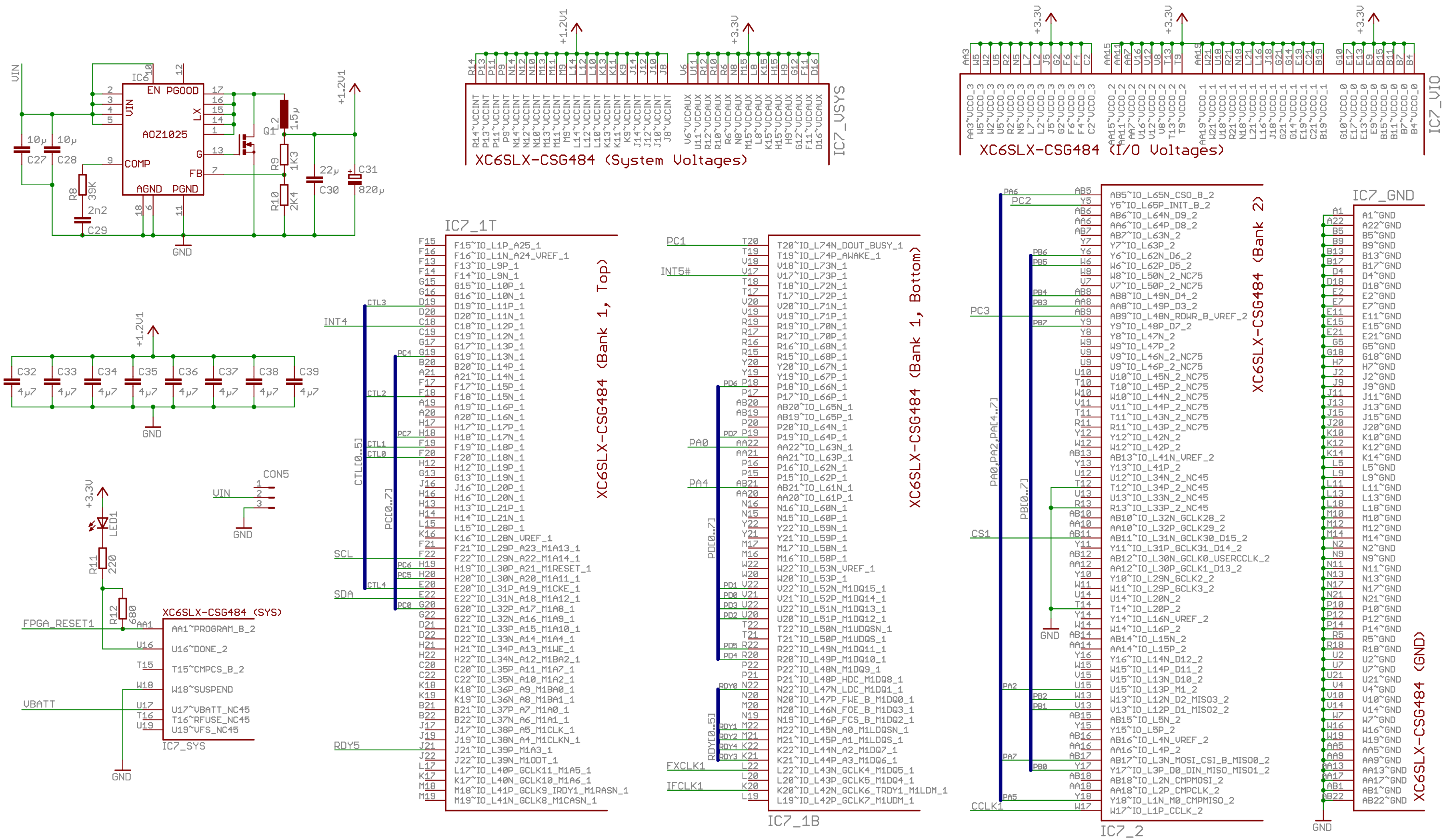
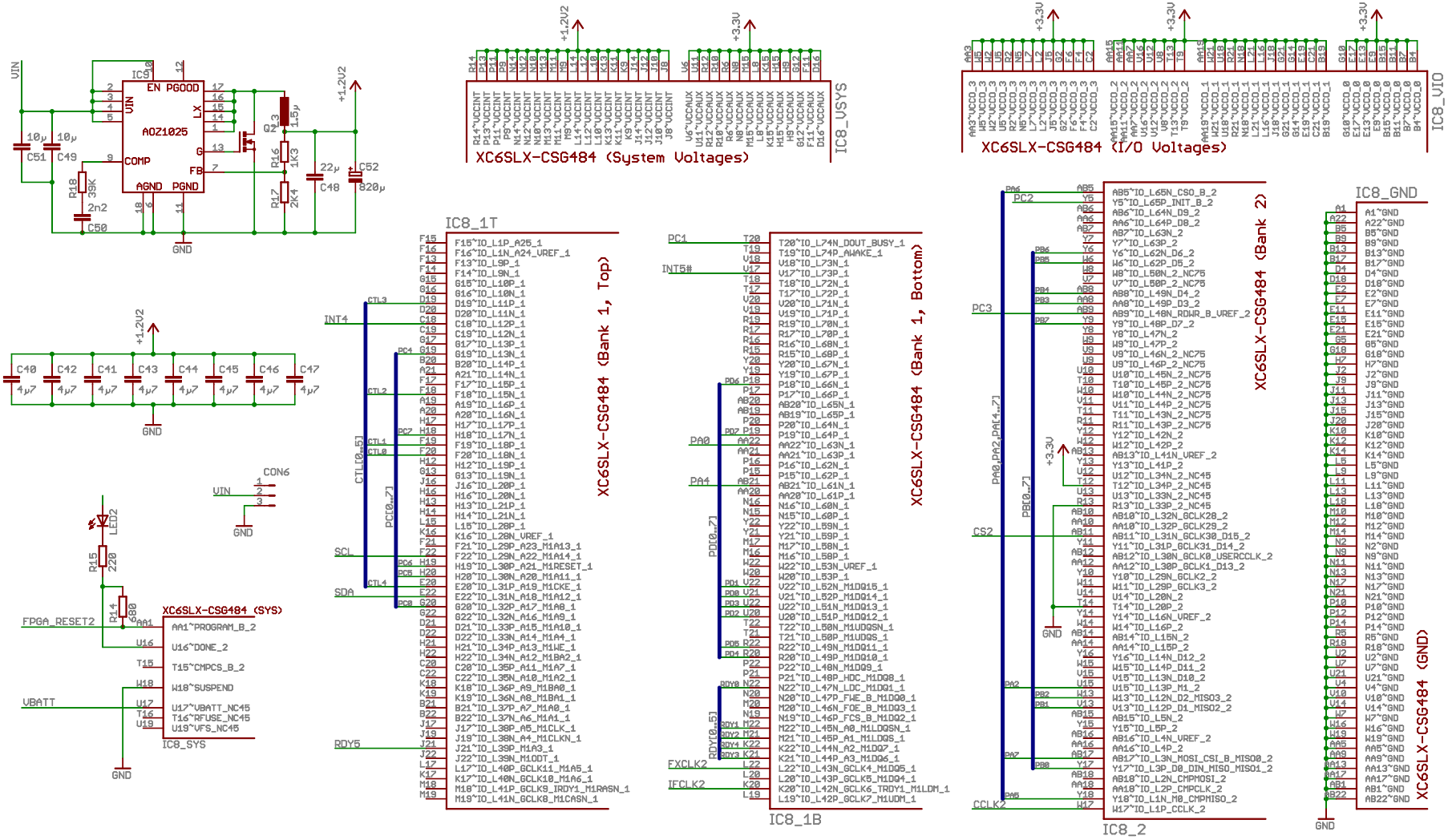
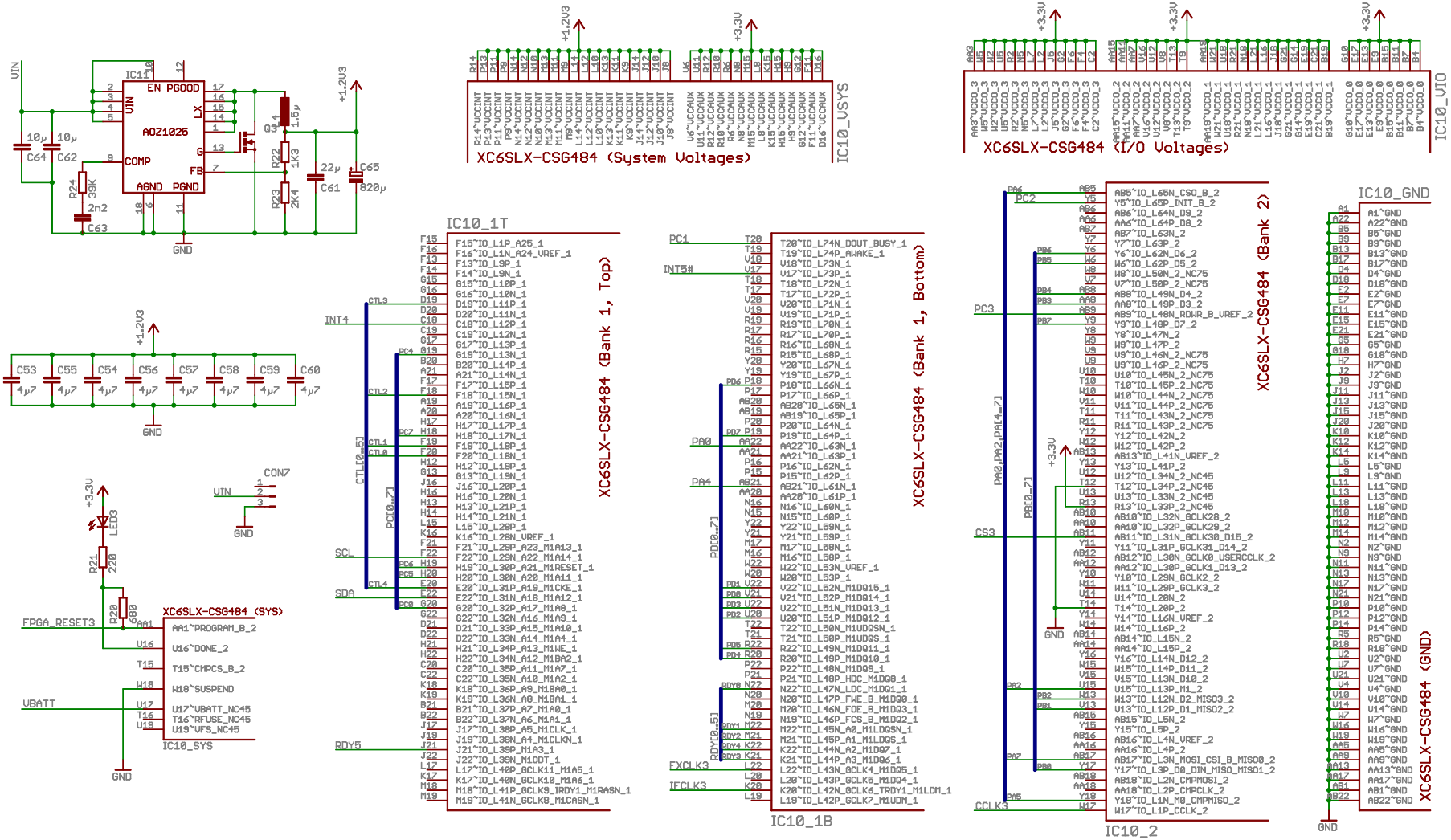
http://www.ztex.de

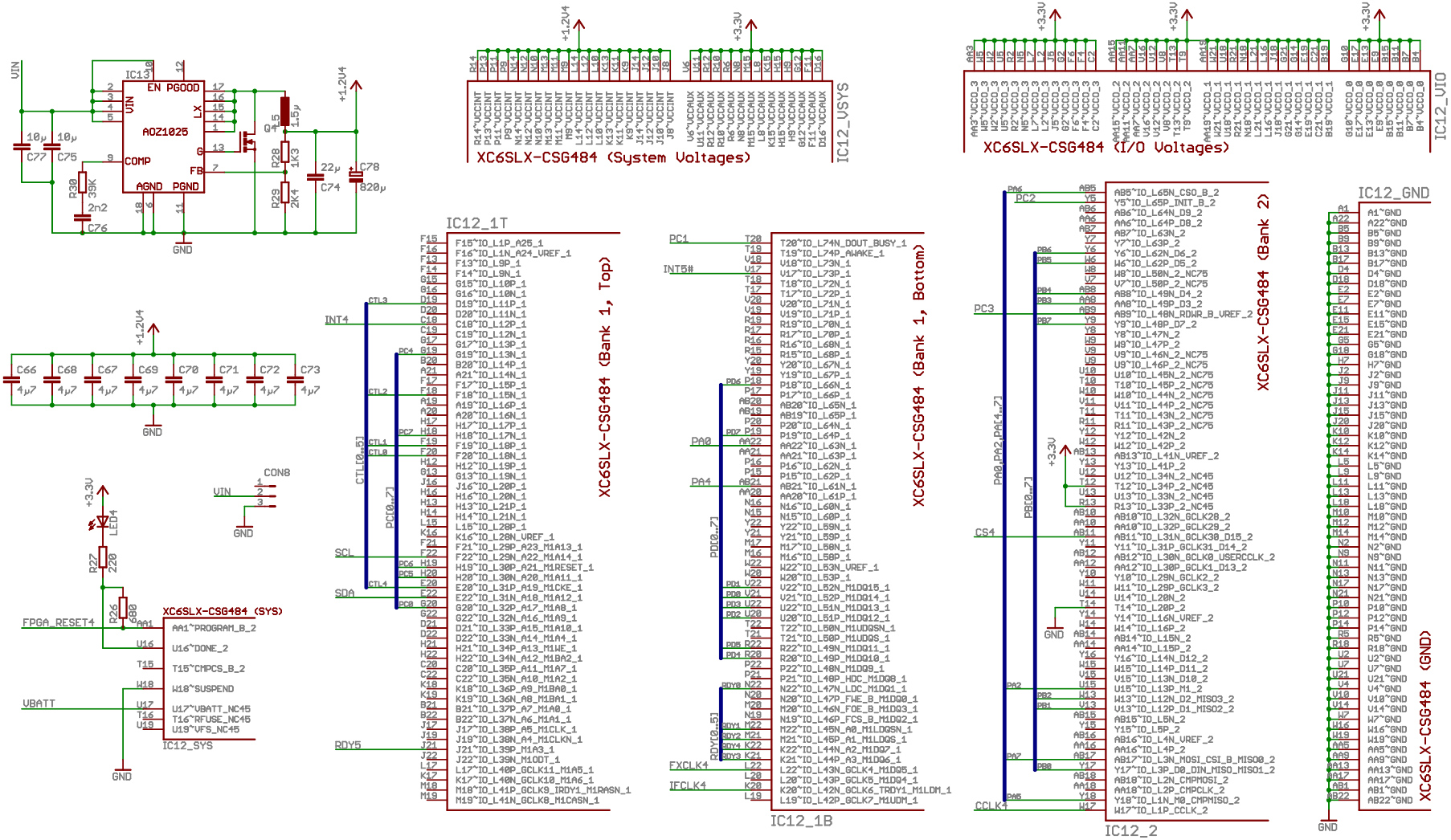

IFCLK
PA0,PA2,PA[4..7]
PROG_GPIF
CCLK
PD[0..7]
PB[0..7]
CTL[0..5]
RDY[0..5]
FX2 (Interface)
IC3_IF
IC3_IO
FX2 (IO)
CON1
+5V
D+
D-
NC
GND
SHD1
SHD2
SHD3
SHD4
XTALOUT
XTALIN
CLKOUT
FXCLK
DPLUS
DMINUS
INT4
INT5#
SCL
SDA
RESET#
*WAKEUP
PC[0..7]
FPGA_RESET1
FPGA_RESET2
FPGA_RESET3
FPGA_RESET4
CS1
CS2
CS3
CS4
24MHz
XTAL1
12p
C2
C1
+3.3V
2K4
R1
R2
R3
IC1
IC2
IC4
VCC
SCL
WP
SDA
A2
A1
A0
Array EEPROM
24LC128SN
24AA025E48/OT
JP1
RST#
MR#
3.08V

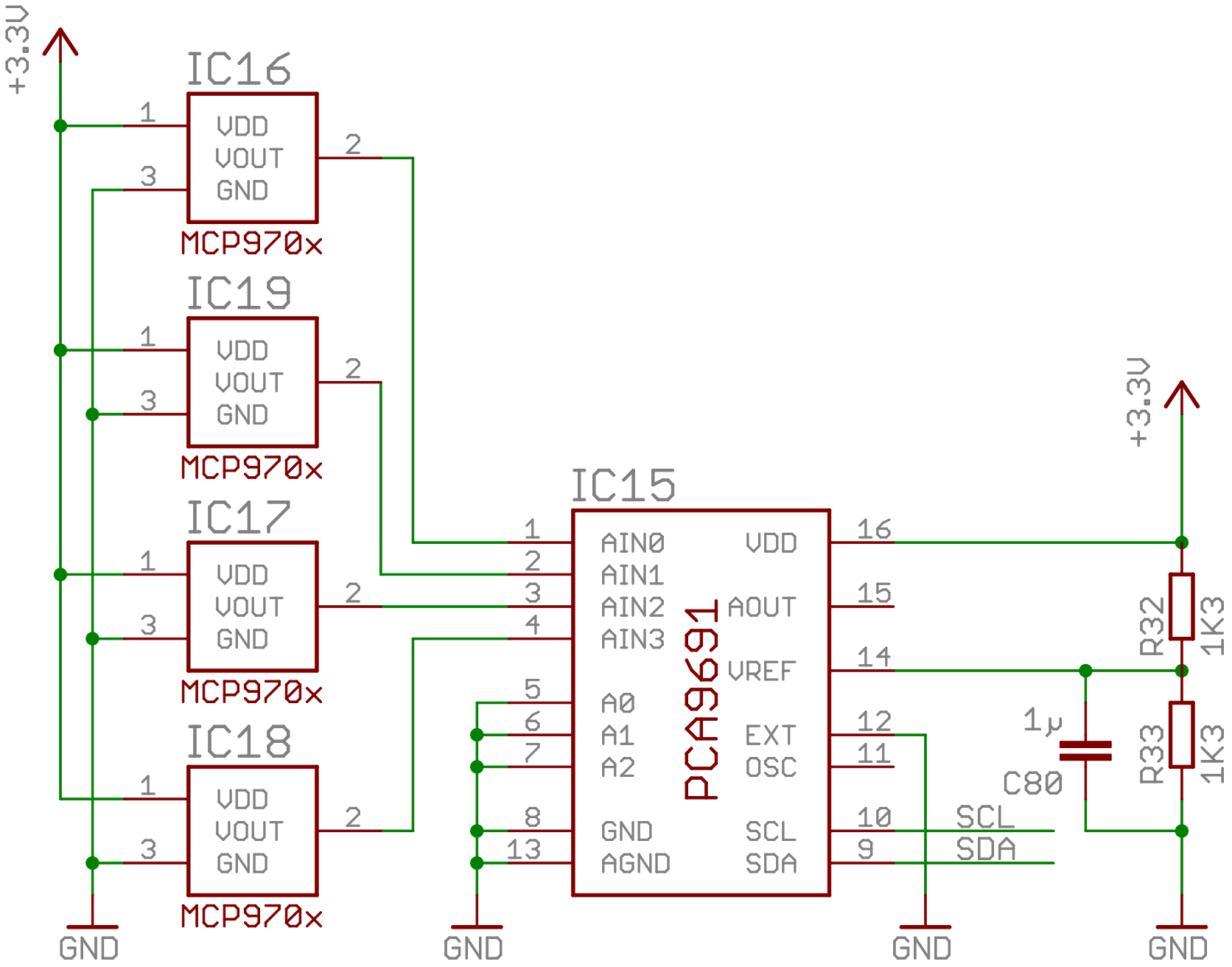


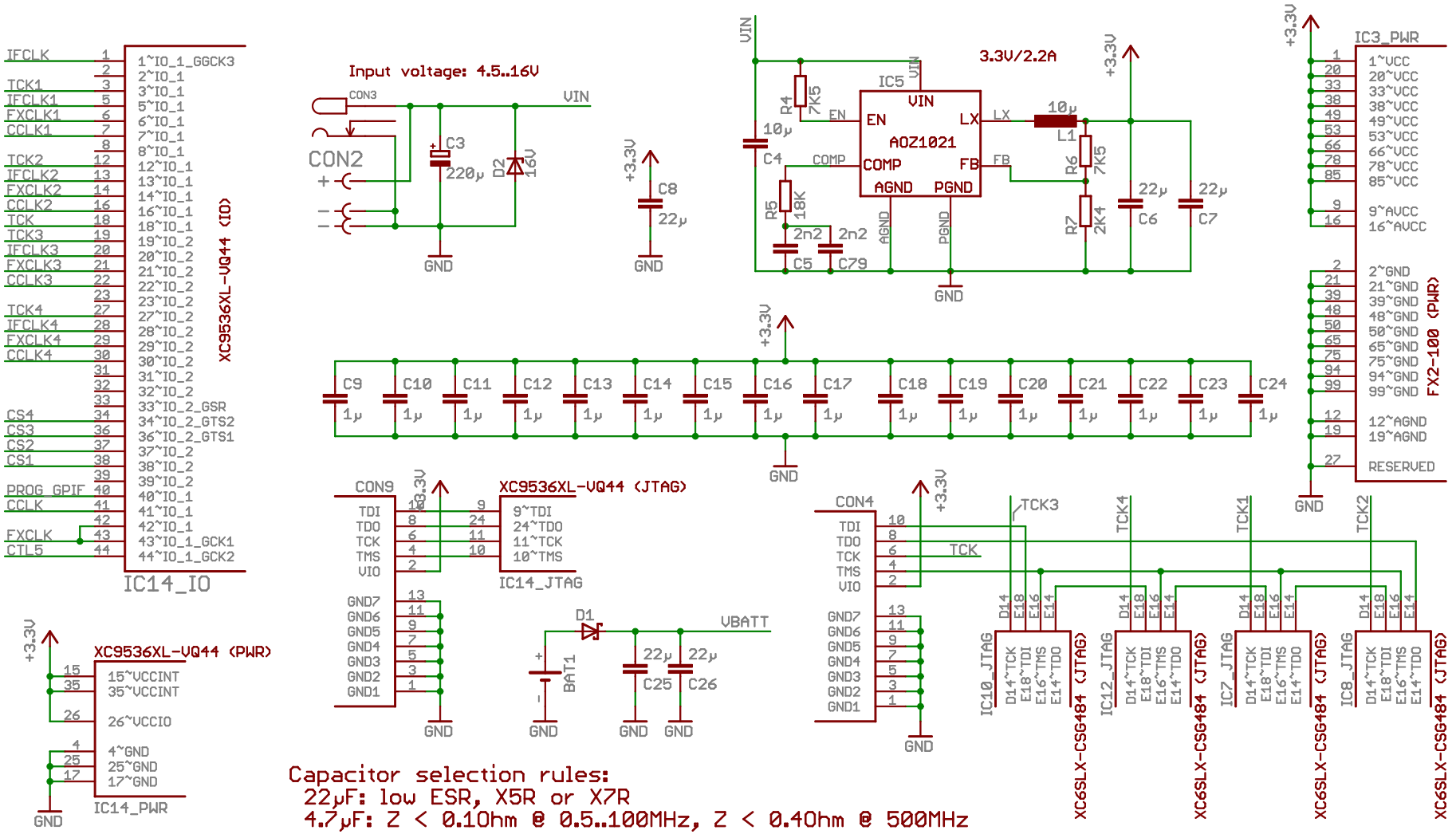
VIN
IC6
AOZ1025
EN PGOOD
VIN
LX
COMP
G
FB
AGND PGND
10µ
C27
10µ
C28
R8
39K
2n2
C29
Q12
15µ
R9
1K3
R10
2K4
22µ
C30
C31
820µ
+1.2V1
GND
C32
C33
C34
C35
C36
C37
C38
C39
4µ7
+3.3V
LED1
R11
220
R12
680
FPGA_RESET1
VBATT
XC6SLX-CSG484 (SYS)
AA1~PROGRAM_B_2
U16~DONE_2
T15~CMPCS_B_2
W18~SUSPEND
U17~VBATT_NC45
T16~RFUSE_NC45
U19~VFS_NC45
IC7_SYS
CON5
VIN
XC6SLX-CSG484 (System Voltages)
IC7_VSYS
+3.3V
XC6SLX-CSG484 (I/O Voltages)
IC7_VIO
IC7_1T
XC6SLX-CSG484 (Bank 1, Top)
INT4
CTL[0..5]
PC[0..7]
SCL
SDA
RDY5
IC7_1B
XC6SLX-CSG484 (Bank 1, Bottom)
PC1
INT5#
PA0
PA4
PD[0..7]
RDY[0..5]
FXCLK1
IFCLK1
IC7_2
XC6SLX-CSG484 (Bank 2)
PC2
PC3
CS1
PA0,PA2,PA[4..7]
PB[0..7]
CCLK1
IC7_GND
XC6SLX-CSG484 (GND)


IC8_1T
XC6SLX-CSG484 (Bank 1, Top)
IC8_1B
XC6SLX-CSG484 (Bank 1, Bottom)
IC8_2
XC6SLX-CSG484 (Bank 2)
IC8_GND
XC6SLX-CSG484 (GND)
IC8_USYS
XC6SLX-CSG484 (System Voltages)
IC8_VIO
XC6SLX-CSG484 (I/O Voltages)
IC8_SYS
XC6SLX-CSG484 (SYS)
AOZ1025
VIN
+1.2V2
+3.3V
GND
FPGA_RESET2
VBATT
SCL
SDA
INT4
INT5#
RDY5
FXCLK2
IFCLK2
PC1
PC2
PC3
PA0
PA4
CS2
CCLK2


IC11
AOZ1025
EN PGOOD
VIN
LX
COMP
FB
AGND PGND
G
VIN
10µ
10µ
C64
C62
R24
39K
2n2
C63
GND
+1.2V3
Q4
1.6µ
R22
1K3
R23
2K4
22µ
C61
C65
820µ
+1.2V3
C53
C55
C54
C56
C57
C58
C59
C60
4µ7
GND
+3.3V
LED3
R21
220
R20
680
FPGA_RESET3
VBATT
XC6SLX-CSG484 (SYS)
AA1~PROGRAM_B_2
U16~DONE_2
T15~CMPCS_B_2
W18~SUSPEND
U17~VBATT_NC45
T16~RFUSE_NC45
U19~VFS_NC45
IC10_SYS
GND
CON7
VIN
GND
+1.2V3
+3.3V
XC6SLX-CSG484 (System Voltages)
IC10_USYS
+3.3V
+3.3V
+3.3V
XC6SLX-CSG484 (I/O Voltages)
IC10_VIO
IC10_1T
XC6SLX-CSG484 (Bank 1, Top)
INT4
SCL
SDA
RDY5
CTL[0..5]
PC[0..7]
IC10_1B
XC6SLX-CSG484 (Bank 1, Bottom)
PC1
INT5#
PA0
PA4
FXCLK3
IFCLK3
PD[0..7]
RDY[0..5]
IC10_2
XC6SLX-CSG484 (Bank 2)
PC3
CS3
CCLK3
PA0,PA2,PA[4..7]
PB[0..7]
IC10_GND
XC6SLX-CSG484 (GND)
GND


IC12_1T
XC6SLX-CSG484 (Bank 1, Top)
IC12_1B
XC6SLX-CSG484 (Bank 1, Bottom)
IC12_2
XC6SLX-CSG484 (Bank 2)
IC12_GND
XC6SLX-CSG484 (GND)
IC12_USYS
XC6SLX-CSG484 (System Voltages)
IC12_VIO
XC6SLX-CSG484 (I/O Voltages)
IC12_SYS
XC6SLX-CSG484 (SYS)
IC13
AOZ1025
EN PGOOD
VIN
COMP
FB
AGND PGND
+1.2V4
+3.3V
GND
CON8
LED4
INT4
INT5#
SCL
SDA
RDY5
FPGA_RESET
VBATT
FXCLK4
IFCLK4
CCLK4
CS4
PC1
PC2
PC3
PA0
PA4
PA2
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7


+3.3V
IC16
VDD
VOUT
GND
MCP970x
IC19
IC17
IC18
IC15
AIN0
AIN1
AIN2
AIN3
A0
A1
A2
GND
AGND
VDD
AOUT
VREF
EXT
OSC
SCL
SDA
PCA9691
R32
1K3
R33
1K3
1µ
C80
SCL
SDA
GND


IC14_IO
XC9536XL-VQ44 (IO)
IC14_PWR
XC9536XL-VQ44 (PWR)
Input voltage: 4.5..16V
CON2
CON3
VIN
GND
3.3V/2.2A
AOZ1021
IC5
IC3_PWR
FX2-100 (PWR)
CON9
XC9536XL-VQ44 (JTAG)
IC14_JTAG
CON4
BAT1
VBATT
TCK3
TCK4
TCK1
TCK2
IC10_JTAG
IC12_JTAG
IC7_JTAG
IC8_JTAG
XC6SLX-CSG484 (JTAG)
Capacitor selection rules:
22µF: low ESR, X5R or X7R
4.7µF: Z < 0.10hm @ 0.5..100MHz, Z < 0.40hm @ 500MHz