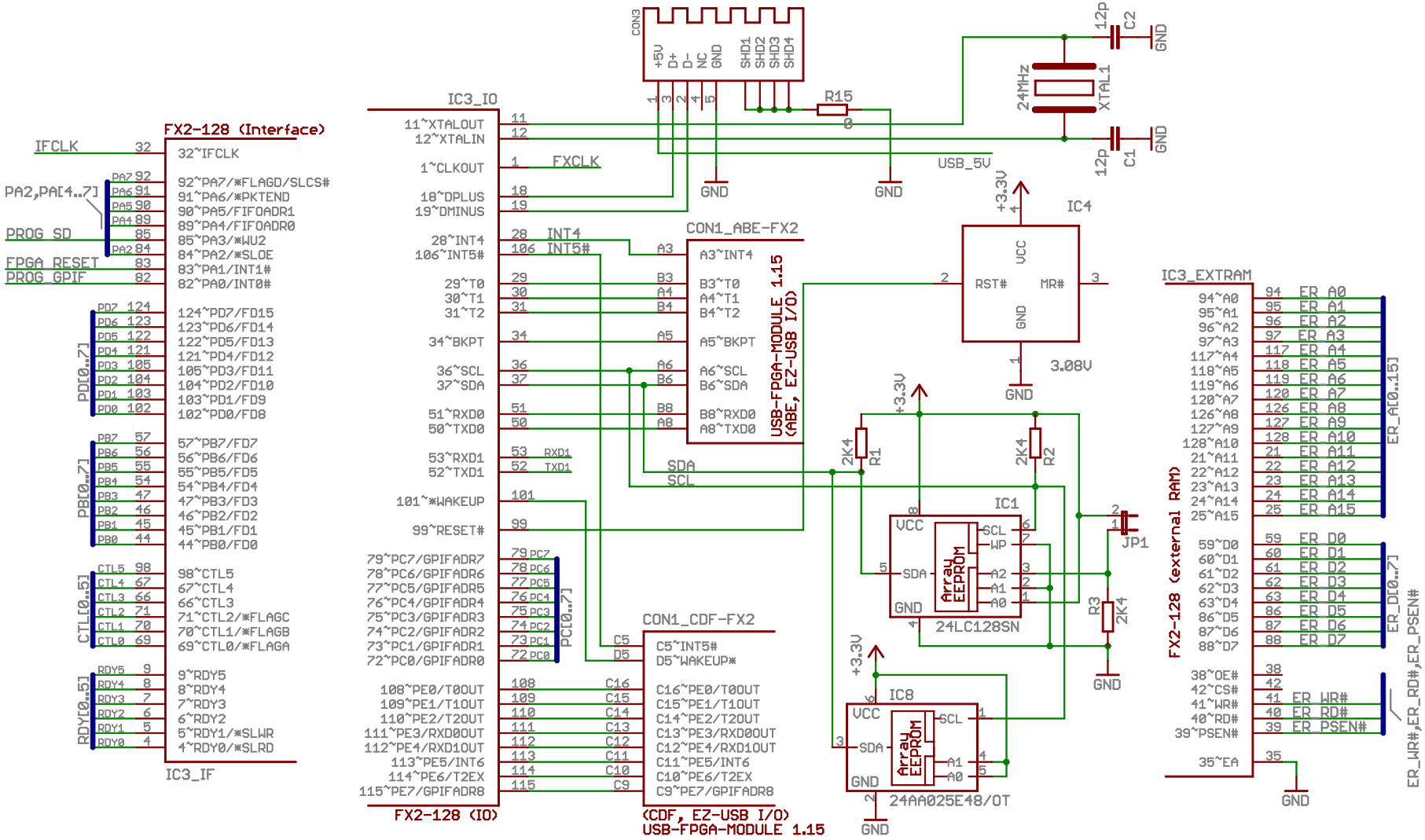
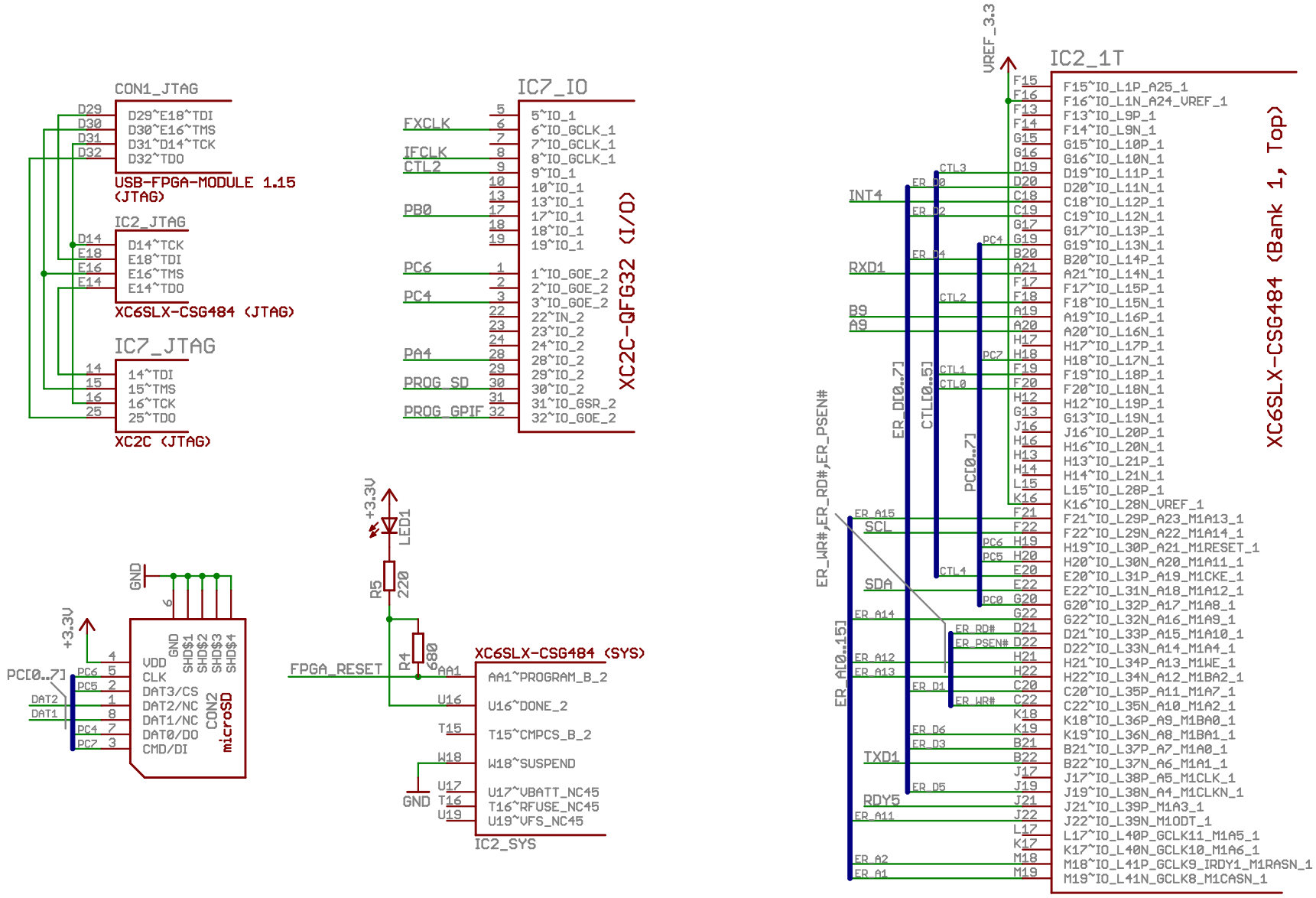
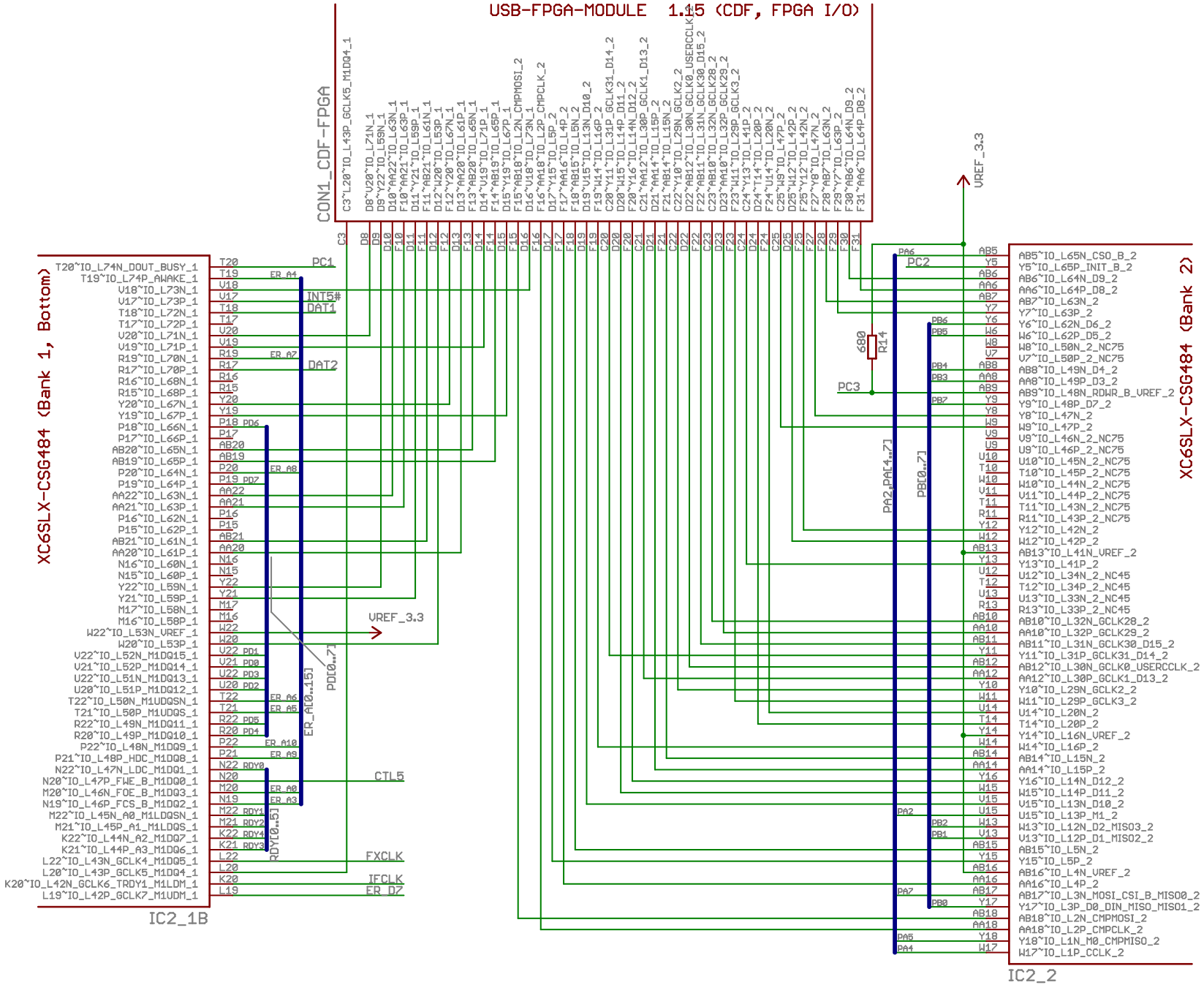
Circuit diagram of ZTEX USB-FPGA-Module 1.15

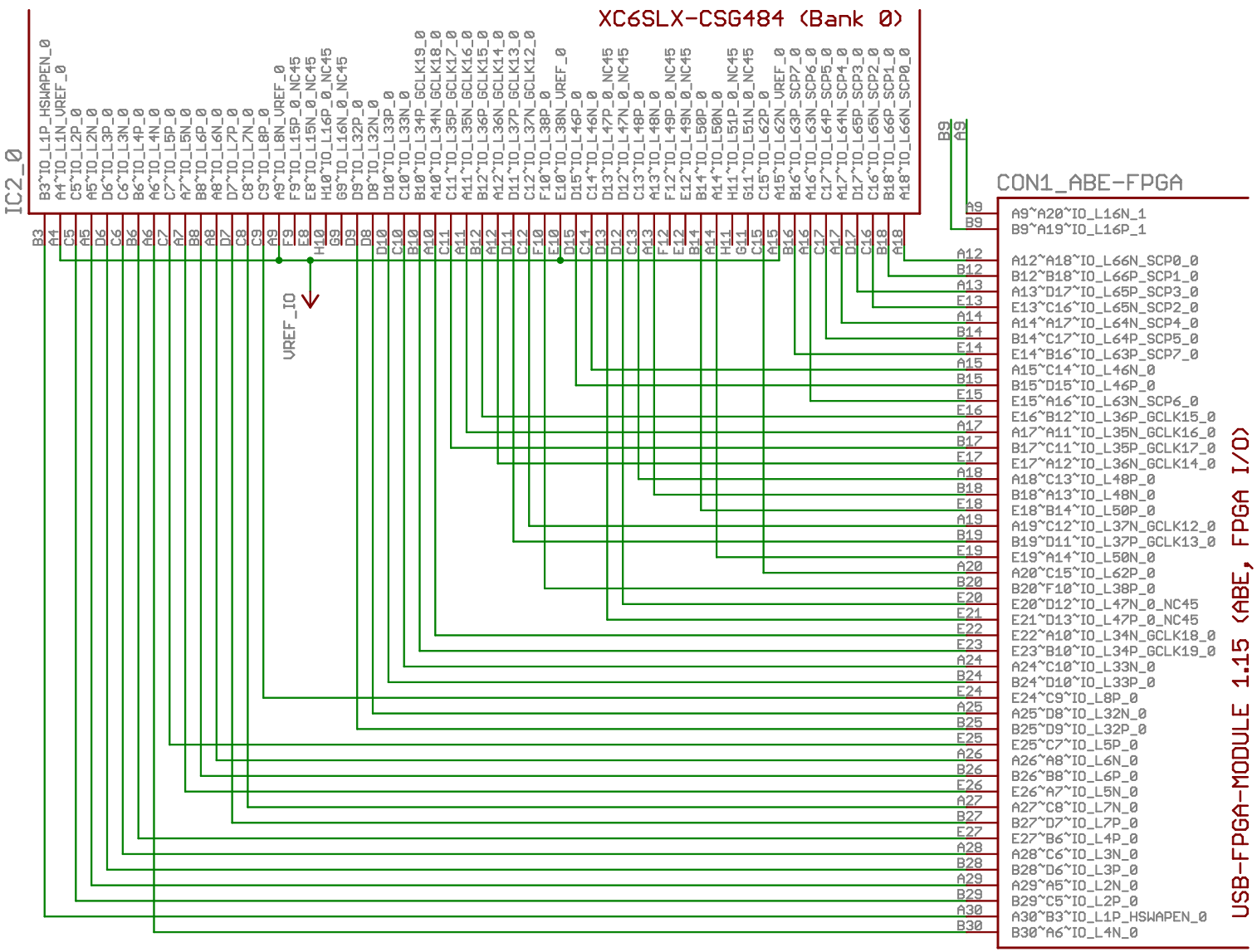
Contents:

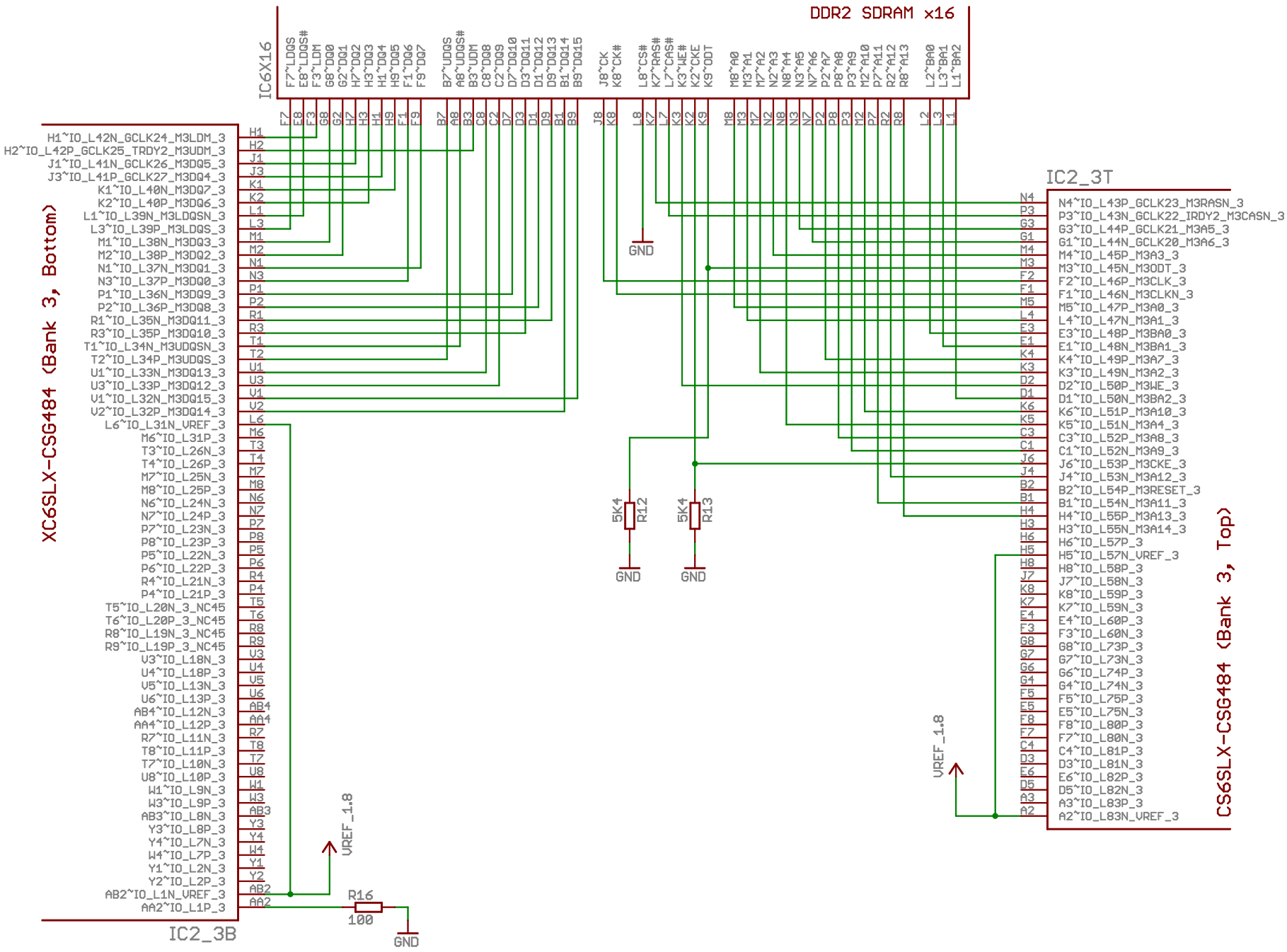
http://www.ztex.de

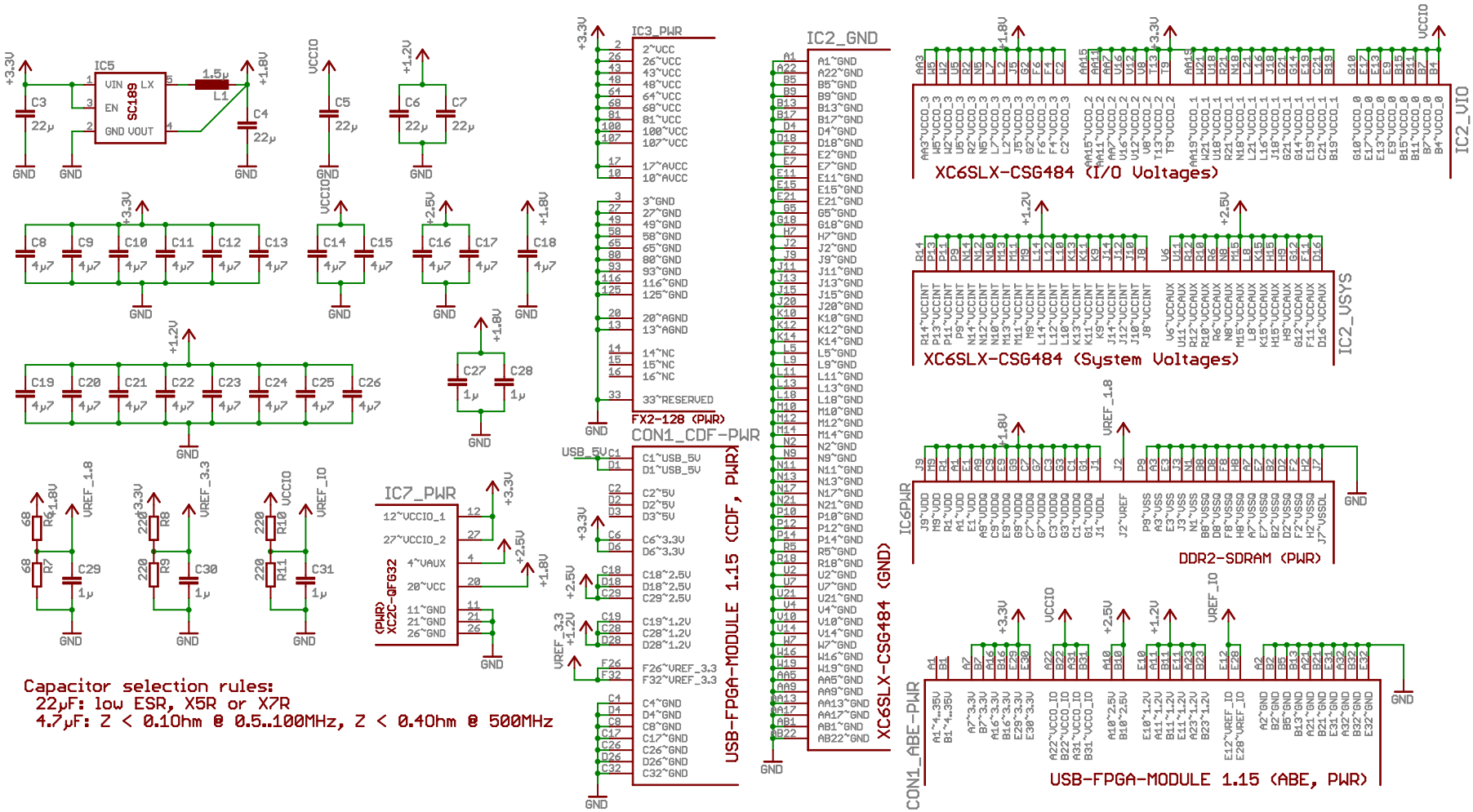

FX2-128 (Interface)
IFCLK
PA2,PA[4..7]
PROG_SD
FPGA_RESET
PROG_GPIF
PD[0..7]
PB[0..7]
CTL[0..5]
RDY[0..5]
IC3_IF
IC3_IO
FX2-128 (IO)
FXCLK
INT4
INT5#
SDA
SCL
RXD1
TXD1
PC[0..7]
CON1_ABE-FX2
USB-FPGA-MODULE 1.15
(ABE, EZ-USB I/O)
CON1_CDF-FX2
(CDF, EZ-USB I/O)
USB-FPGA-MODULE 1.15
CON3
+5V
D+
D-
NC
GND
SHD1
SHD2
SHD3
SHD4
R15
0
24MHz
XTAL1
12p
C2
C1
USB_5V
IC4
VCC
RST#
MR#
GND
3.08V
+3.3V
2K4
R1
R2
R3
IC1
IC8
Array EEPROM
24LC128SN
24AA025E48/OT
JP1
IC3_EXTRAM
FX2-128 (external RAM)
ER_A[0..15]
ER_D[0..7]
ER_WR#,ER_RD#,ER_PSEN#


CON1_JTAG
D29
D30
D31
D32
D29~E18~TDI
D30~E16~TMS
D31~D14~TCK
D32~TDO
USB-FPGA-MODULE 1.15
(JTAG)
IC2_JTAG
D14
E18
E16
E14
D14~TCK
E18~TDI
E16~TMS
E14~TDO
XC6SLX-CSG484 (JTAG)
IC7_JTAG
14
15
16
25
14~TDI
15~TMS
16~TCK
25~TDO
XC2C (JTAG)
IC7_IO
FXCLK
IFCLK
CTL2
PB0
PC6
PC4
PA4
PROG_SD
PROG_GPIF
5~IO_1
6~IO_GCLK_1
7~IO_GCLK_1
8~IO_GCLK_1
9~IO_1
10~IO_1
13~IO_1
17~IO_1
18~IO_1
19~IO_1
1~IO_GOE_2
2~IO_GOE_2
3~IO_GOE_2
22~IN_2
23~IO_2
24~IO_2
28~IO_2
29~IO_2
30~IO_2
31~IO_GSR_2
32~IO_GOE_2
XC2C-QFG32 (I/O)
VREF_3.3
IC2_1T
INT4
RXD1
B9
A9
TXD1
RDY5
SCL
SDA
ER_DI[0..7]
CTL[0..5]
PC[0..7]
ER_WR#,ER_RD#,ER_PSEN#
ER_A[0..15]
F15~IO_L1P_A25_1
F16~IO_L1N_A24_VREF_1
F13~IO_L9P_1
F14~IO_L9N_1
G15~IO_L10P_1
G16~IO_L10N_1
D19~IO_L11P_1
D20~IO_L11N_1
C18~IO_L12P_1
C19~IO_L12N_1
G17~IO_L13P_1
G19~IO_L13N_1
B20~IO_L14P_1
A21~IO_L14N_1
F17~IO_L15P_1
F18~IO_L15N_1
A19~IO_L16P_1
A20~IO_L16N_1
H17~IO_L17P_1
H18~IO_L17N_1
F19~IO_L18P_1
F20~IO_L18N_1
H12~IO_L19P_1
G13~IO_L19N_1
J16~IO_L20P_1
H16~IO_L20N_1
H13~IO_L21P_1
H14~IO_L21N_1
L15~IO_L28P_1
K16~IO_L28N_VREF_1
F21~IO_L29P_A23_M1A13_1
F22~IO_L29N_A22_M1A14_1
H19~IO_L30P_A21_M1RESET_1
H20~IO_L30N_A20_M1A11_1
E20~IO_L31P_A19_M1CKE_1
E22~IO_L31N_A18_M1A12_1
G20~IO_L32P_A17_M1A8_1
G22~IO_L32N_A16_M1A9_1
D21~IO_L33P_A15_M1A10_1
D22~IO_L33N_A14_M1A4_1
H21~IO_L34P_A13_M1WE_1
H22~IO_L34N_A12_M1BA2_1
C20~IO_L35P_A11_M1A7_1
C22~IO_L35N_A10_M1A2_1
K18~IO_L36P_A9_M1BA0_1
K19~IO_L36N_A8_M1BA1_1
B21~IO_L37P_A7_M1A0_1
B22~IO_L37N_A6_M1A1_1
J17~IO_L38P_A5_M1CLK_1
J19~IO_L38N_A4_M1CLKN_1
J21~IO_L39P_M1A3_1
J22~IO_L39N_M1ODT_1
L17~IO_L40P_GCLK11_M1A5_1
K17~IO_L40N_GCLK10_M1A6_1
M18~IO_L41P_GCLK9_IRDY1_M1RASN_1
M19~IO_L41N_GCLK8_M1CASN_1
XC6SLX-CSG484 (Bank 1, Top)
+3.3V
LED1
R5
220
GND
FPGA_RESET
R4
680
XC6SLX-CSG484 (SYS)
AA1~PROGRAM_B_2
U16~DONE_2
T15~CMPCS_B_2
W18~SUSPEND
U17~VBATT_NC45
T16~RFUSE_NC45
U19~VFS_NC45
IC2_SYS
PC[0..7]
DAT2
DAT1
VDD
CLK
DAT3/CS
DAT2/NC
DAT1/NC
DAT0/DO
CMD/DI
GND
SHD$1
SHD$2
SHD$3
SHD$4
CON2
microSD


USB-FPGA-MODULE 1.15 (CDF, FPGA I/O)
CON1_CDF-FPGA
XC6SLX-CSG484 (Bank 1, Bottom)
IC2_1B
XC6SLX-CSG484 (Bank 2)
IC2_2
VREF_3.3
PC1
PC2
PC3
INT5#
DAT1
DAT2
CTL5
FXCLK
IFCLK
FLAGD
680
R14


XC6SLX-CSG484 (Bank 0)
IC2_0
B3~IO_L1P_HSWAPEN_0
A4~IO_L1N_VREF_0
C5~IO_L2P_0
A5~IO_L2N_0
D6~IO_L3P_0
C6~IO_L3N_0
B6~IO_L4P_0
A6~IO_L4N_0
C7~IO_L5P_0
A7~IO_L5N_0
B8~IO_L6P_0
A8~IO_L6N_0
D7~IO_L7P_0
C8~IO_L7N_0
C9~IO_L8P_0
A9~IO_L8N_VREF_0
F9~IO_L15P_0_NC45
E8~IO_L15N_0_NC45
H10~IO_L16P_0_NC45
G9~IO_L16N_0_NC45
D9~IO_L32P_0
D8~IO_L32N_0
D10~IO_L33P_0
C10~IO_L33N_0
B10~IO_L34P_GCLK19_0
A10~IO_L34N_GCLK18_0
C11~IO_L35P_GCLK17_0
A11~IO_L35N_GCLK16_0
B12~IO_L36P_GCLK15_0
A12~IO_L36N_GCLK14_0
D11~IO_L37P_GCLK13_0
C12~IO_L37N_GCLK12_0
F10~IO_L38P_0
E10~IO_L38N_VREF_0
D15~IO_L46P_0
C14~IO_L46N_0
D13~IO_L47P_0_NC45
D12~IO_L47N_0_NC45
C13~IO_L48P_0
A13~IO_L48N_0
F12~IO_L49P_0_NC45
E12~IO_L49N_0_NC45
B14~IO_L50P_0
A14~IO_L50N_0
H11~IO_L51P_0_NC45
G11~IO_L51N_0_NC45
C15~IO_L62P_0
A15~IO_L62N_VREF_0
B16~IO_L63P_SCP7_0
A16~IO_L63N_SCP6_0
C17~IO_L64P_SCP5_0
A17~IO_L64N_SCP4_0
D17~IO_L65P_SCP3_0
C16~IO_L65N_SCP2_0
B18~IO_L66P_SCP1_0
A18~IO_L66N_SCP0_0
VREF_IO
B9
A9
CON1_ABE-FPGA
A9~A20~IO_L16N_1
B9~A19~IO_L16P_1
A12~A18~IO_L66N_SCP0_0
B12~B18~IO_L66P_SCP1_0
A13~D17~IO_L65P_SCP3_0
E13~C16~IO_L65N_SCP2_0
A14~A17~IO_L64N_SCP4_0
B14~C17~IO_L64P_SCP5_0
E14~B16~IO_L63P_SCP7_0
A15~C14~IO_L46N_0
B15~D15~IO_L46P_0
E15~A16~IO_L63N_SCP6_0
E16~B12~IO_L36P_GCLK15_0
A17~A11~IO_L35N_GCLK16_0
B17~C11~IO_L35P_GCLK17_0
E17~A12~IO_L36N_GCLK14_0
A18~C13~IO_L48P_0
B18~A13~IO_L48N_0
E18~B14~IO_L50P_0
A19~C12~IO_L37N_GCLK12_0
B19~D11~IO_L37P_GCLK13_0
E19~A14~IO_L50N_0
A20~C15~IO_L62P_0
B20~F10~IO_L38P_0
E20~D12~IO_L47N_0_NC45
E21~D13~IO_L47P_0_NC45
E22~A10~IO_L34N_GCLK18_0
E23~B10~IO_L34P_GCLK19_0
A24~C10~IO_L33N_0
B24~D10~IO_L33P_0
E24~C9~IO_L8P_0
A25~D8~IO_L32N_0
B25~D9~IO_L32P_0
E25~C7~IO_L5P_0
A26~A8~IO_L6N_0
B26~B8~IO_L6P_0
E26~A7~IO_L5N_0
A27~C8~IO_L7N_0
B27~D7~IO_L7P_0
E27~B6~IO_L4P_0
A28~C6~IO_L3N_0
B28~D6~IO_L3P_0
A29~A5~IO_L2N_0
B29~C5~IO_L2P_0
A30~B3~IO_L1P_HSWAPEN_0
B30~A6~IO_L4N_0
USB-FPGA-MODULE 1.15 (ABE, FPGA I/O)


DDR2 SDRAM x16
IC6X16
XC6SLX-CSG484 (Bank 3, Bottom)
IC2_3B
IC2_3T
CS6SLX-CSG484 (Bank 3, Top)
5K4
R12
5K4
R13
R16
100
VREF_1.8
VREF_1.8
GND
GND
GND
GND


IC5
SC189
VIN
LX
EN
GND VOUT
L1
1.5µ
C3
22µ
C4
22µ
C5
22µ
C6
22µ
C7
22µ
C8
4µ7
C9
4µ7
C10
4µ7
C11
4µ7
C12
4µ7
C13
4µ7
C14
4µ7
C15
4µ7
C16
4µ7
C17
4µ7
C18
4µ7
C19
4µ7
C20
4µ7
C21
4µ7
C22
4µ7
C23
4µ7
C24
4µ7
C25
4µ7
C26
4µ7
C27
1µ
C28
1µ
R6
68
R7
68
C29
1µ
R8
220
R9
220
C30
1µ
R10
220
R11
220
C31
1µ
IC7_PWR
12~VCCIO_1
27~VCCIO_2
4~VAUX
20~VCC
11~GND
21~GND
26~GND
(PWR)
XC2C-QFG32
IC3_PWR
2~VCC
26~VCC
43~VCC
48~VCC
64~VCC
68~VCC
81~VCC
100~VCC
107~VCC
17~AVCC
10~AVCC
3~GND
27~GND
49~GND
58~GND
65~GND
80~GND
93~GND
116~GND
125~GND
20~AGND
13~AGND
14~NC
15~NC
16~NC
33~RESERVED
FX2-128 (PWR)
CON1_CDF-PWR
C1~USB_5V
D1~USB_5V
C2~5V
D2~5V
D3~5V
C6~3.3V
D6~3.3V
C18~2.5V
D18~2.5V
C29~2.5V
C19~1.2V
C28~1.2V
D28~1.2V
F26~VREF_3.3
F32~VREF_3.3
C4~GND
D4~GND
C8~GND
C17~GND
C26~GND
D26~GND
C32~GND
USB-FPGA-MODULE 1.15 (CDF, PWR)
IC2_GND
A1~GND
A22~GND
B5~GND
B9~GND
B13~GND
B17~GND
D4~GND
D18~GND
E2~GND
E7~GND
E11~GND
E15~GND
E21~GND
G5~GND
G18~GND
H7~GND
J2~GND
J9~GND
J11~GND
J13~GND
J15~GND
J20~GND
K10~GND
K12~GND
K14~GND
L5~GND
L9~GND
L11~GND
L13~GND
L18~GND
M10~GND
M12~GND
M14~GND
N2~GND
N9~GND
N11~GND
N13~GND
N17~GND
N21~GND
P10~GND
P12~GND
P14~GND
R5~GND
R18~GND
U2~GND
U7~GND
U21~GND
V4~GND
V10~GND
V14~GND
W7~GND
W16~GND
W19~GND
AA5~GND
AA9~GND
AA13~GND
AA17~GND
AB1~GND
AB22~GND
XC6SLX-CSG484 (GND)
IC2_VIO
XC6SLX-CSG484 (I/O Voltages)
IC2_VSYS
XC6SLX-CSG484 (System Voltages)
IC6PWR
DDR2-SDRAM (PWR)
CON1_ABE-PWR
USB-FPGA-MODULE 1.15 (ABE, PWR)
Capacitor selection rules:
22µF: low ESR, X5R or X7R
4.7µF: Z < 0.10ohm @ 0.5..100MHz, Z < 0.40ohm @ 500MHz