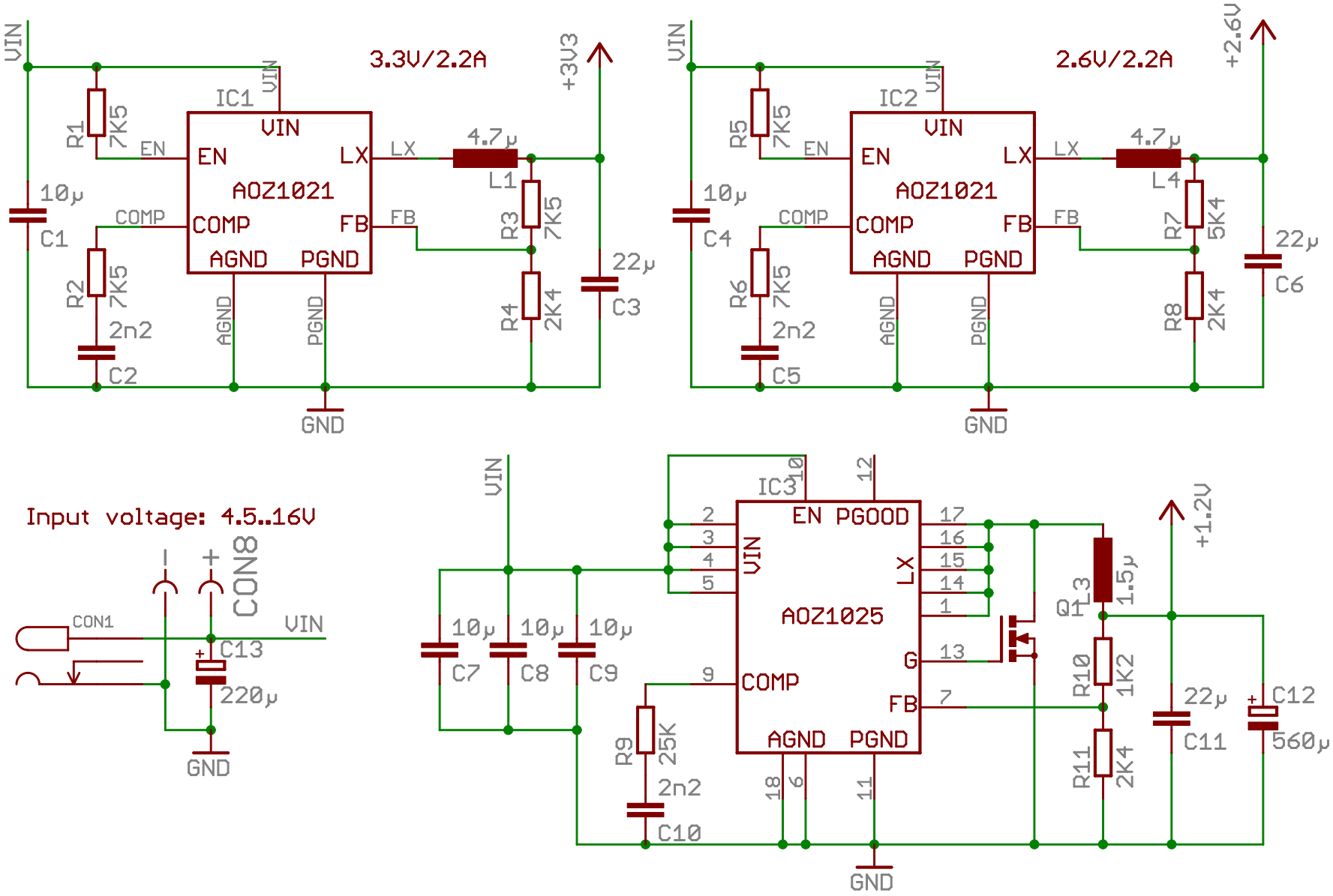
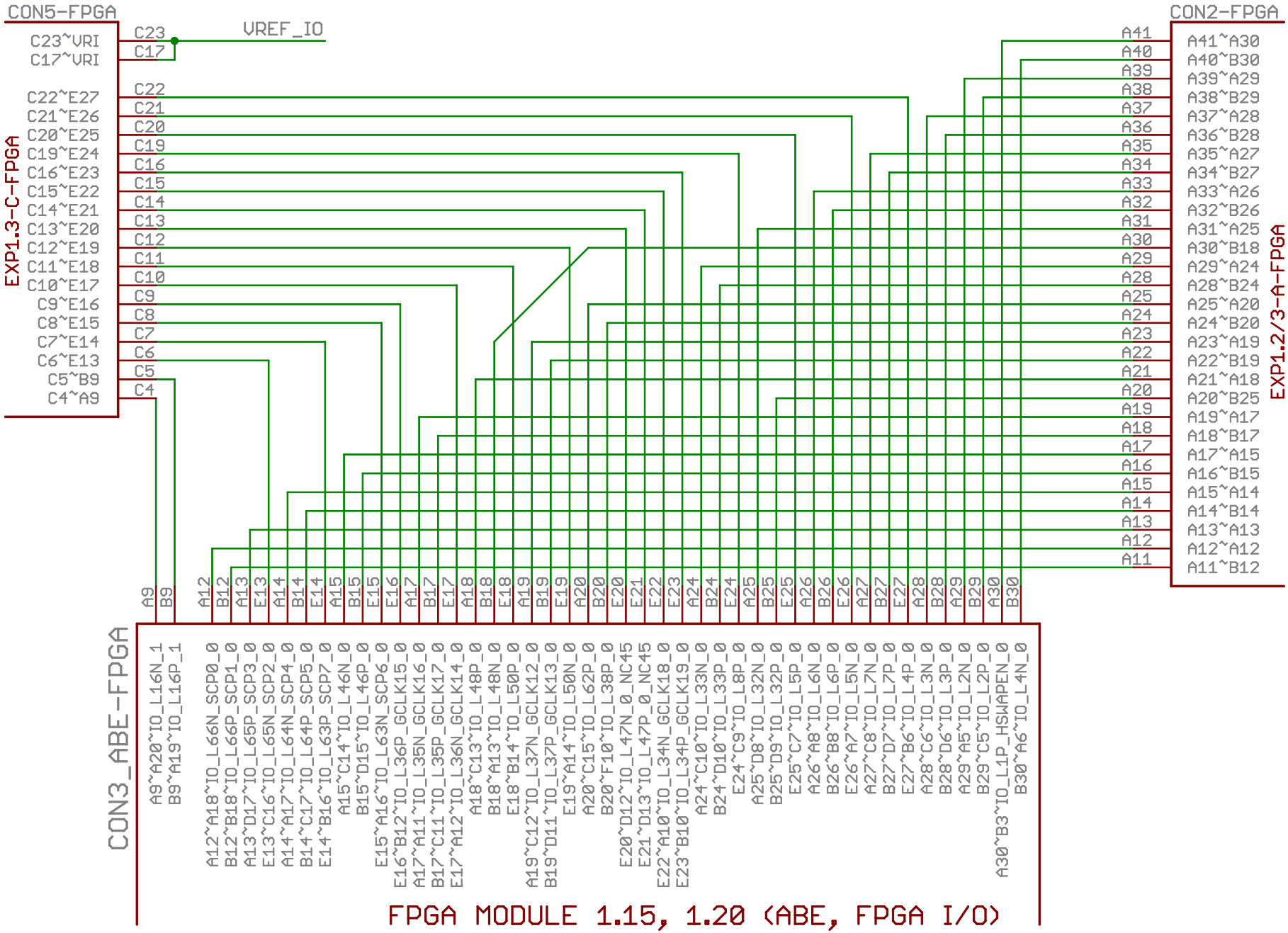
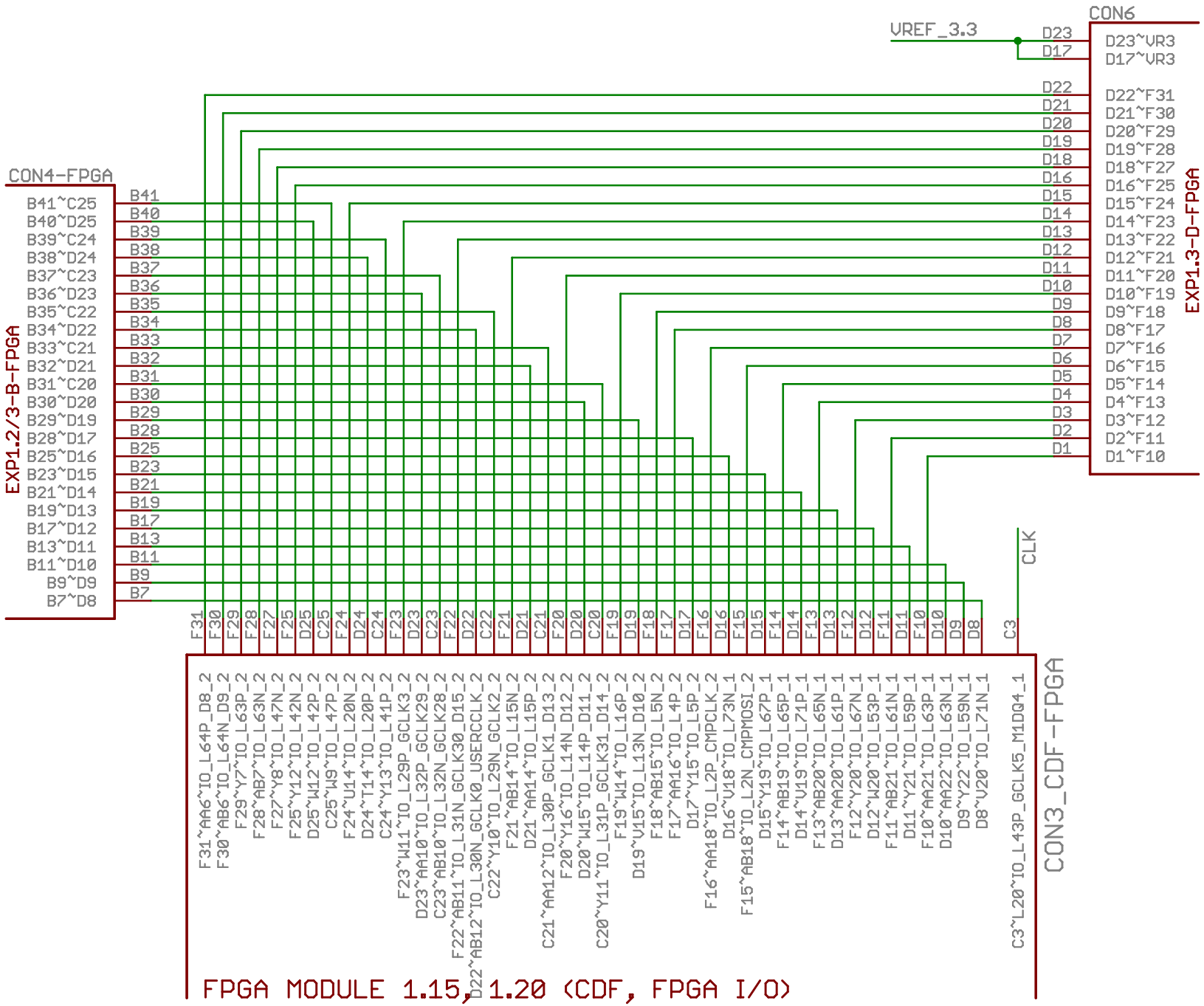
Circuit diagram of ZTEX Experimental Board 1.3

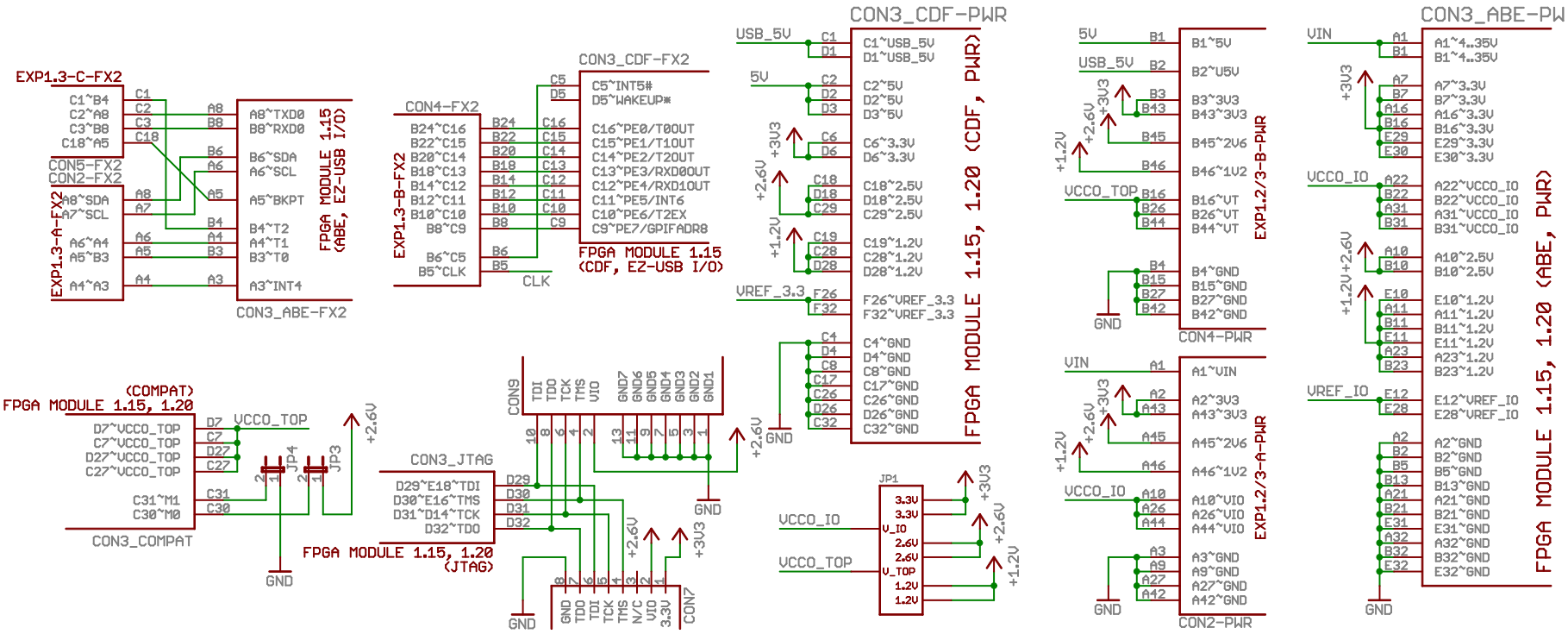
Contents:

http://www.ztex.de


3.3V/2.2A
IC1
AOZ1021
VIN
EN
LX
COMP
FB
AGND
PGND
R1 7K5
R2 7K5
R3 7K5
R4 2K4
C1 10µ
C2 2n2
C3 22µ
L1 4.7µ
+3V3
GND
2.6V/2.2A
IC2
R5 7K5
R6 7K5
R7 5K4
R8 2K4
C4 10µ
C5 2n2
C6 22µ
L4 4.7µ
+2.6V
Input voltage: 4.5..16V
CON8
CON1
C13 220µ
IC3
AOZ1025
PGOOD
G
C7 10µ
C8 10µ
C9 10µ
R9 25K
C10 2n2
Q1
L3 1.5µ
R10 1K2
R11 2K4
C11 22µ
C12 560µ
+1.2V


CON5-FPGA
EXP1.3-C-FPGA
C23~VRI
C17~VRI
C22~E27
C21~E26
C20~E25
C19~E24
C16~E23
C15~E22
C14~E21
C13~E20
C12~E19
C11~E18
C10~E17
C9~E16
C8~E15
C7~E14
C6~E13
C5~B9
C4~A9
C23
C17
C22
C21
C20
C19
C16
C15
C14
C13
C12
C11
C10
C9
C8
C7
C6
C5
C4
VREF_IO
CON2-FPGA
EXP1.2/3-A-FPGA
A41
A40
A39
A38
A37
A36
A35
A34
A33
A32
A31
A30
A29
A28
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A15
A14
A13
A12
A11
A41~A30
A40~B30
A39~A29
A38~B29
A37~A28
A36~B28
A35~A27
A34~B27
A33~A26
A32~B26
A31~A25
A30~B18
A29~A24
A28~B24
A25~A20
A24~B20
A23~A19
A22~B19
A21~A18
A20~B25
A19~A17
A18~B17
A17~A15
A16~B15
A15~A14
A14~B14
A13~A13
A12~A12
A11~B12
CON3_ABE-FPGA
A9 B9 A12 B12 A13 E13 A14 B14 E14 A15 B15 E15 E16 A17 B17 E17 A18 B18 E18 A19 B19 E19 A20 B20 E20 E21 E22 E23 A24 B24 E24 A25 B25 E25 A26 B26 E26 A27 B27 E27 A28 B28 A29 B29 A30 B30
A9~A20~IO_L16N_1
B9~A19~IO_L16P_1
A12~A18~IO_L66N_SCP0_0
B12~B18~IO_L66P_SCP1_0
A13~D17~IO_L65P_SCP3_0
E13~C16~IO_L65N_SCP2_0
A14~A17~IO_L64N_SCP4_0
B14~C17~IO_L64P_SCP5_0
E14~B16~IO_L63P_SCP7_0
A15~C14~IO_L46N_0
B15~D15~IO_L46P_0
E15~A16~IO_L63N_SCP6_0
E16~B12~IO_L36P_GCLK15_0
A17~A11~IO_L35N_GCLK16_0
B17~C11~IO_L35P_GCLK17_0
E17~A12~IO_L36N_GCLK14_0
A18~C13~IO_L48P_0
B18~A13~IO_L48N_0
E18~B14~IO_L50P_0
A19~C12~IO_L37N_GCLK12_0
B19~D11~IO_L37P_GCLK13_0
E19~A14~IO_L50N_0
A20~C15~IO_L62P_0
B20~F10~IO_L38P_0
E20~D12~IO_L47N_0_NC45
E21~D13~IO_L47P_0_NC45
E22~A10~IO_L34N_GCLK18_0
E23~B10~IO_L34P_GCLK19_0
A24~C10~IO_L33N_0
B24~D10~IO_L33P_0
E24~C9~IO_L8P_0
A25~D8~IO_L32N_0
B25~D9~IO_L32P_0
E25~C7~IO_L5P_0
A26~A8~IO_L6N_0
B26~B8~IO_L6P_0
E26~A7~IO_L5N_0
A27~C8~IO_L7N_0
B27~D7~IO_L7P_0
E27~B6~IO_L4P_0
A28~C6~IO_L3N_0
B28~D6~IO_L3P_0
A29~A5~IO_L2N_0
B29~C5~IO_L2P_0
A30~B3~IO_L1P_HSWAPEN_0
B30~A6~IO_L4N_0
FPGA MODULE 1.15, 1.20 (ABE, FPGA I/O)


CON6
VREF_3.3
D23
D17
D22
D21
D20
D19
D18
D16
D15
D14
D13
D12
D11
D10
D9
D8
D7
D6
D5
D4
D3
D2
D1
D23~VR3
D17~VR3
D22~F31
D21~F30
D20~F29
D19~F28
D18~F27
D16~F25
D15~F24
D14~F23
D13~F22
D12~F21
D11~F20
D10~F19
D9~F18
D8~F17
D7~F16
D6~F15
D5~F14
D4~F13
D3~F12
D2~F11
D1~F10
EXP1.3-D-FPGA
CON4-FPGA
B41~C25
B40~D25
B39~C24
B38~D24
B37~C23
B36~D23
B35~C22
B34~D22
B33~C21
B32~D21
B31~C20
B30~D20
B29~D19
B28~D17
B25~D16
B23~D15
B21~D14
B19~D13
B17~D12
B13~D11
B11~D10
B9~D9
B7~D8
B41
B40
B39
B38
B37
B36
B35
B34
B33
B32
B31
B30
B29
B28
B25
B23
B21
B19
B17
B13
B11
B9
B7
EXP1.2/3-B-FPGA
CLK
C3
F31
F30
F29
F28
F27
F25
D25
C25
F24
D24
C24
F23
D23
C23
F22
D22
C22
F21
D21
C21
F20
D20
C20
F19
D19
F18
F17
D17
F16
D16
F15
D15
F14
D14
F13
D12
D11
F10
D10
D9
D8
F31~AA6~IO_L64P_D8_2
F30~AB6~IO_L64N_D9_2
F29~Y7~IO_L63P_2
F28~AB7~IO_L63N_2
F27~Y8~IO_L47N_2
F25~Y12~IO_L42N_2
D25~W12~IO_L42P_2
C25~W9~IO_L47P_2
F24~U14~IO_L20N_2
D24~T14~IO_L20P_2
C24~Y13~IO_L41P_2
F23~W11~IO_L29P_GCLK3_2
D23~AA10~IO_L32P_GCLK29_2
C23~AB10~IO_L32N_GCLK28_2
F22~AB11~IO_L31N_GCLK30_D15_2
D22~AB12~IO_L30N_GCLK0_USERCCLK_2
C22~Y10~IO_L29N_GCLK2_2
F21~AB14~IO_L15N_2
D21~AA14~IO_L15P_2
C21~AA12~IO_L30P_GCLK1_D13_2
F20~Y16~IO_L14N_D12_2
D20~W15~IO_L14P_D11_2
C20~Y11~IO_L31P_GCLK31_D14_2
F19~W14~IO_L16P_2
D19~V15~IO_L13N_D10_2
F18~AB15~IO_L5N_2
F17~AA16~IO_L4P_2
D17~Y15~IO_L5P_2
F16~AA18~IO_L2P_CMPCLK_2
D16~V18~IO_L73N_1
F15~AB18~IO_L2N_CMPMOSI_2
D15~Y19~IO_L67P_1
F14~AB19~IO_L65P_1
D14~V19~IO_L71P_1
F13~AB20~IO_L65N_1
D13~AA20~IO_L61P_1
F12~Y20~IO_L67N_1
D12~W20~IO_L53P_1
F11~AB21~IO_L61N_1
D11~Y21~IO_L59P_1
F10~AA21~IO_L63P_1
D10~AA22~IO_L63N_1
D9~Y22~IO_L59N_1
D8~V20~IO_L71N_1
C3~L20~IO_L43P_GCLK5_M1DQ4_1
CON3_CDF-FPGA
FPGA MODULE 1.15, 1.20 (CDF, FPGA I/O)


EXP1.3-C-FX2
C1~B4
C2~A8
C3~B8
C18~A5
CON5-FX2
CON2-FX2
EXP1.3-A-FX2
A8~SDA
A7~SCL
A6~A4
A5~B3
A4~A3
A8~TXD0
B8~RXD0
B6~SDA
A6~SCL
A5~BKPT
B4~T2
A4~T1
B3~T0
A3~INT4
FPGA MODULE 1.15 (ABE, EZ-USB I/O)
CON3_ABE-FX2
CON3_CDF-FX2
CON4-FX2
EXP1.3-B-FX2
B24~C16
B22~C15
B20~C14
B18~C13
B14~C12
B12~C11
B10~C10
B8~C9
B6~C5
B5~CLK
C5~INT5#
D5~WAKEUP*
C16~PE0/T0OUT
C15~PE1/T1OUT
C14~PE2/T2OUT
C13~PE3/RXD0OUT
C12~PE4/RXD1OUT
C11~PE5/INT6
C10~PE6/T2EX
C9~PE7/GPIFADR8
CLK
FPGA MODULE 1.15 (CDF, EZ-USB I/O)
CON3_CDF-PWR
USB_5V
5V
+3V3
+2.6V
+1.2V
VREF_3.3
C1~USB_5V
D1~USB_5V
C2~5V
D2~5V
D3~5V
C6~3.3V
D6~3.3V
C18~2.5V
D18~2.5V
C29~2.5V
C19~1.2V
C28~1.2V
D28~1.2V
F26~VREF_3.3
F32~VREF_3.3
C4~GND
D4~GND
C8~GND
C17~GND
C26~GND
D26~GND
C32~GND
FPGA MODULE 1.15, 1.20 (CDF, PWR)
(COMPAT)
FPGA MODULE 1.15, 1.20
D7~VCCO_TOP
C7~VCCO_TOP
D27~VCCO_TOP
C27~VCCO_TOP
C31~M1
C30~M0
CON3_COMPAT
VCCO_TOP
JP4
JP3
CON3_JTAG
D29~E18~TDI
D30~E16~TMS
D31~D14~TCK
D32~TDO
FPGA MODULE 1.15, 1.20 (JTAG)
CON9
TDI
TDO
TCK
TMS
VIO
GND7
GND6
GND5
GND4
GND3
GND2
GND1
CON7
GND
N/C
3.3V
JP1
3.3V
V_IO
2.6V
V_TOP
1.2V
VCCO_IO
VCCO_TOP
5V
USB_5V
B1~5V
B2~U5V
B3~3V3
B43~3V3
B45~2V6
B46~1V2
B16~VT
B26~VT
B44~VT
B4~GND
B15~GND
B27~GND
B42~GND
EXP1.2/3-B-PWR
CON4-PWR
VIN
A1~VIN
A2~3V3
A43~3V3
A45~2V6
A46~1V2
A10~VIO
A26~VIO
A44~VIO
A3~GND
A9~GND
A27~GND
A42~GND
EXP1.2/3-A-PWR
CON2-PWR
CON3_ABE-PW
A1~4..35V
B1~4..35V
A7~3.3V
B7~3.3V
A16~3.3V
B16~3.3V
E29~3.3V
E30~3.3V
A22~VCCO_IO
B22~VCCO_IO
A31~VCCO_IO
B31~VCCO_IO
A10~2.5V
B10~2.5V
E10~1.2V
A11~1.2V
B11~1.2V
E11~1.2V
A23~1.2V
B23~1.2V
VREF_IO
E12~VREF_IO
E28~VREF_IO
A2~GND
B2~GND
B5~GND
B13~GND
A21~GND
B21~GND
E31~GND
A32~GND
B32~GND
E32~GND
FPGA MODULE 1.15, 1.20 (ABE, PWR)