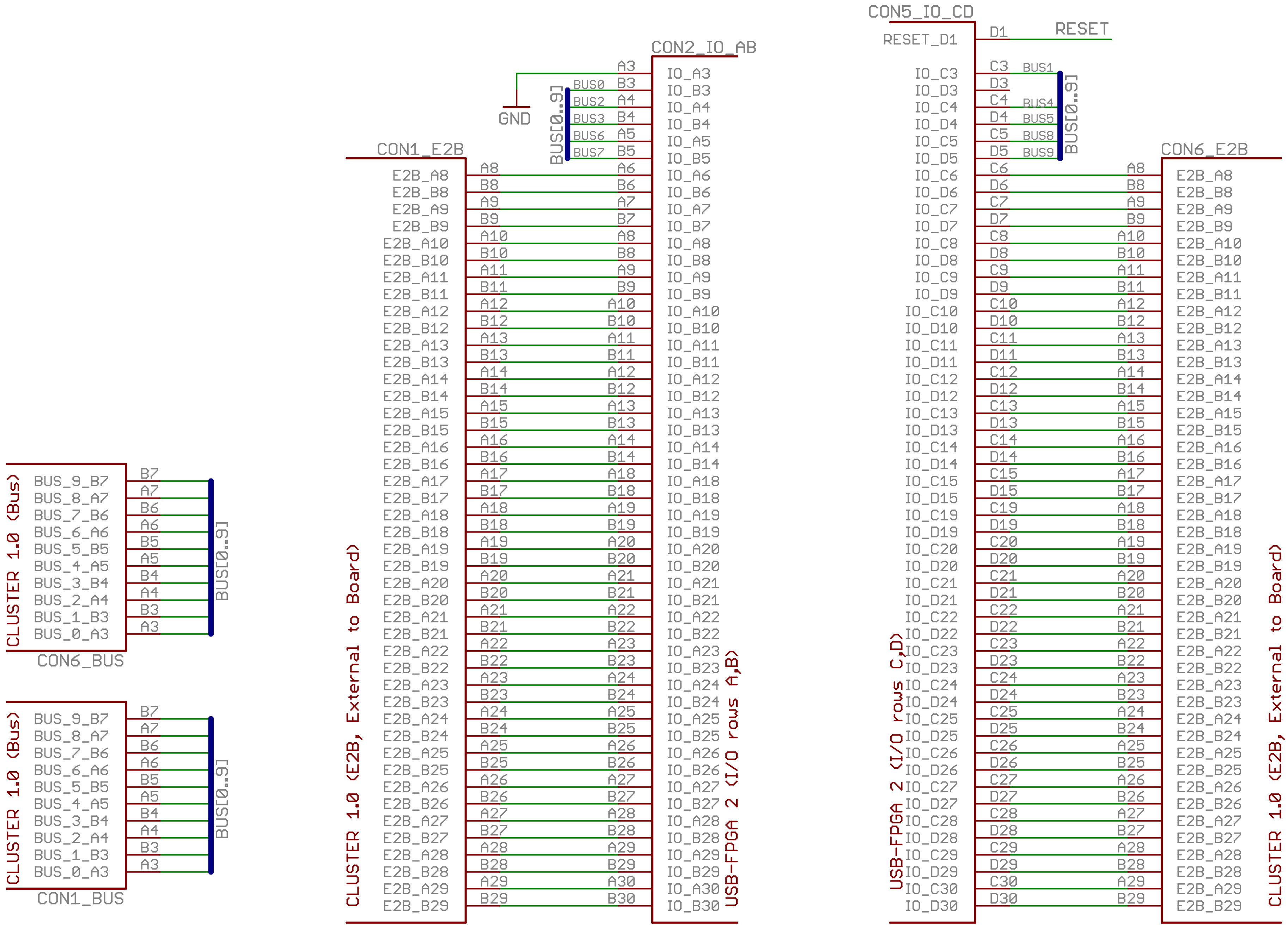
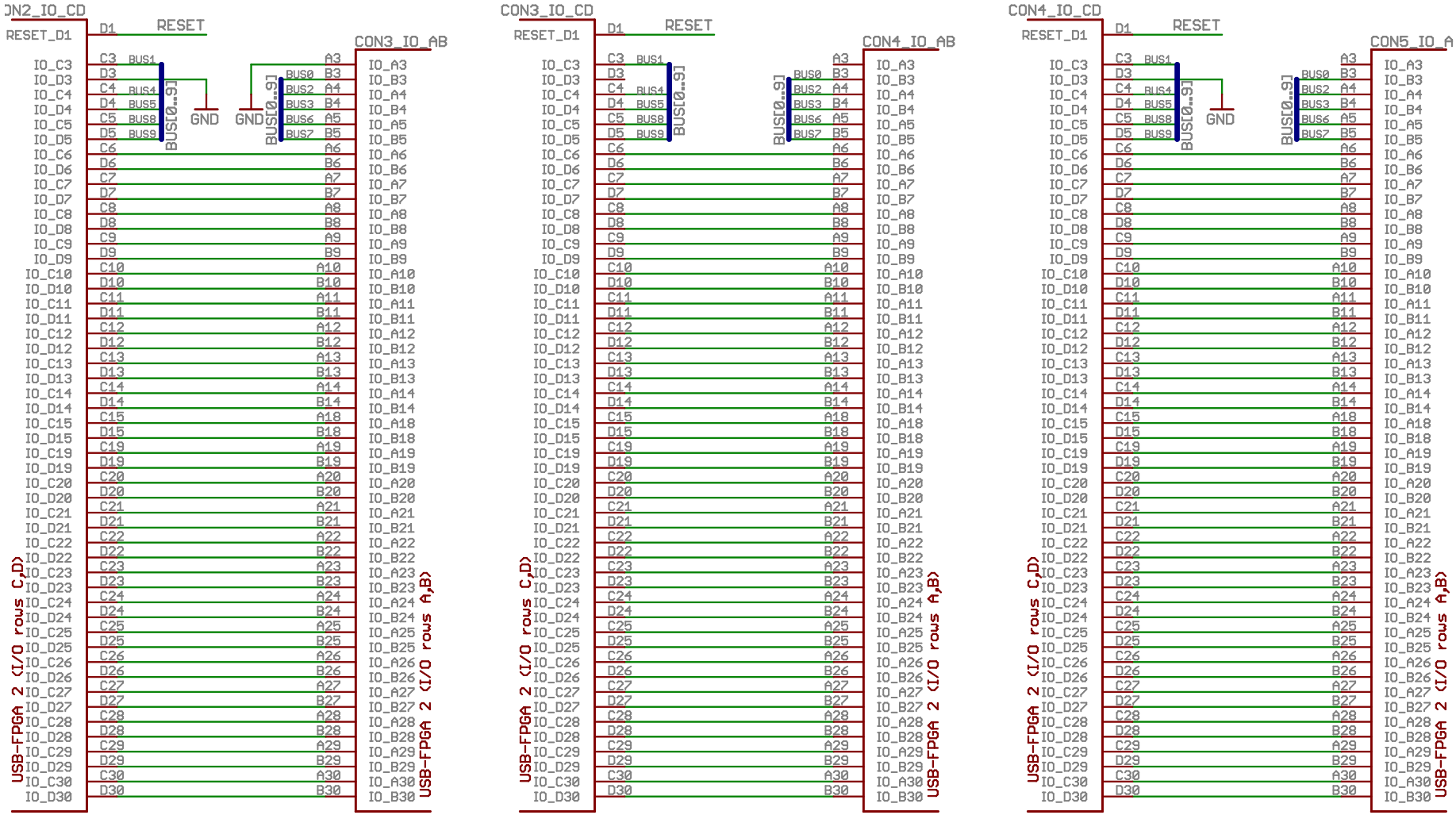
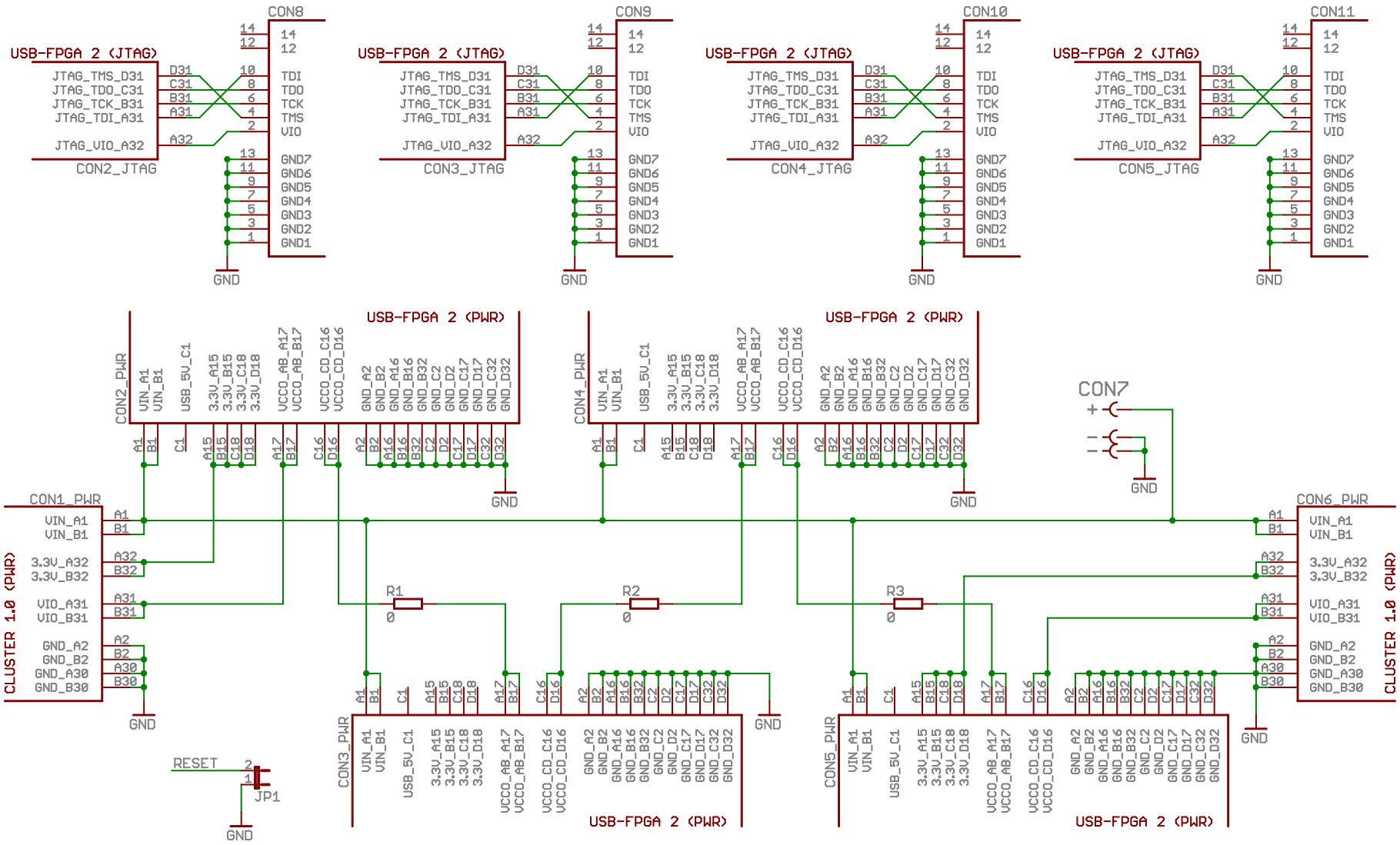
Circuit diagram of Cluster Base Board for ZTEX Series 2 FPGA Boards

Contents:

http://www.ztex.de


CON2_IO_AB
CON5_IO_CD
CON1_E2B
CON6_E2B
CON6_BUS
CON1_BUS
GND
RESET
RESET_D1
D1
BUS[0..9]
BUS0
BUS1
BUS2
BUS3
BUS4
BUS5
BUS6
BUS7
BUS8
BUS9
BUS_9_B7
BUS_8_A7
BUS_7_B6
BUS_6_A6
BUS_5_B5
BUS_4_A5
BUS_3_B4
BUS_2_A4
BUS_1_B3
BUS_0_A3
CLUSTER 1.0 (Bus)
CLUSTER 1.0 (E2B, External to Board)
USB-FPGA 2 (I/O rows A,B)
USB-FPGA 2 (I/O rows C,D)
IO_A3 … IO_B30
IO_C3 … IO_D30
E2B_A8 … E2B_B29


CON2_IO_CD
RESET_D1
D1
RESET
CON3_IO_AB
BUS1
BUS4
BUS5
BUS8
BUS9
BUS[0..9]
GND
BUS0
BUS2
BUS3
BUS6
BUS7
USB-FPGA 2 (I/O rows C,D)
USB-FPGA 2 (I/O rows A,B)
CON3_IO_CD
CON4_IO_AB
CON4_IO_CD
CON5_IO_A



R0, R1 and R2 are not installed by default