Circuit diagram of ZTEX USB-FPGA-Module 1.11

Contents:

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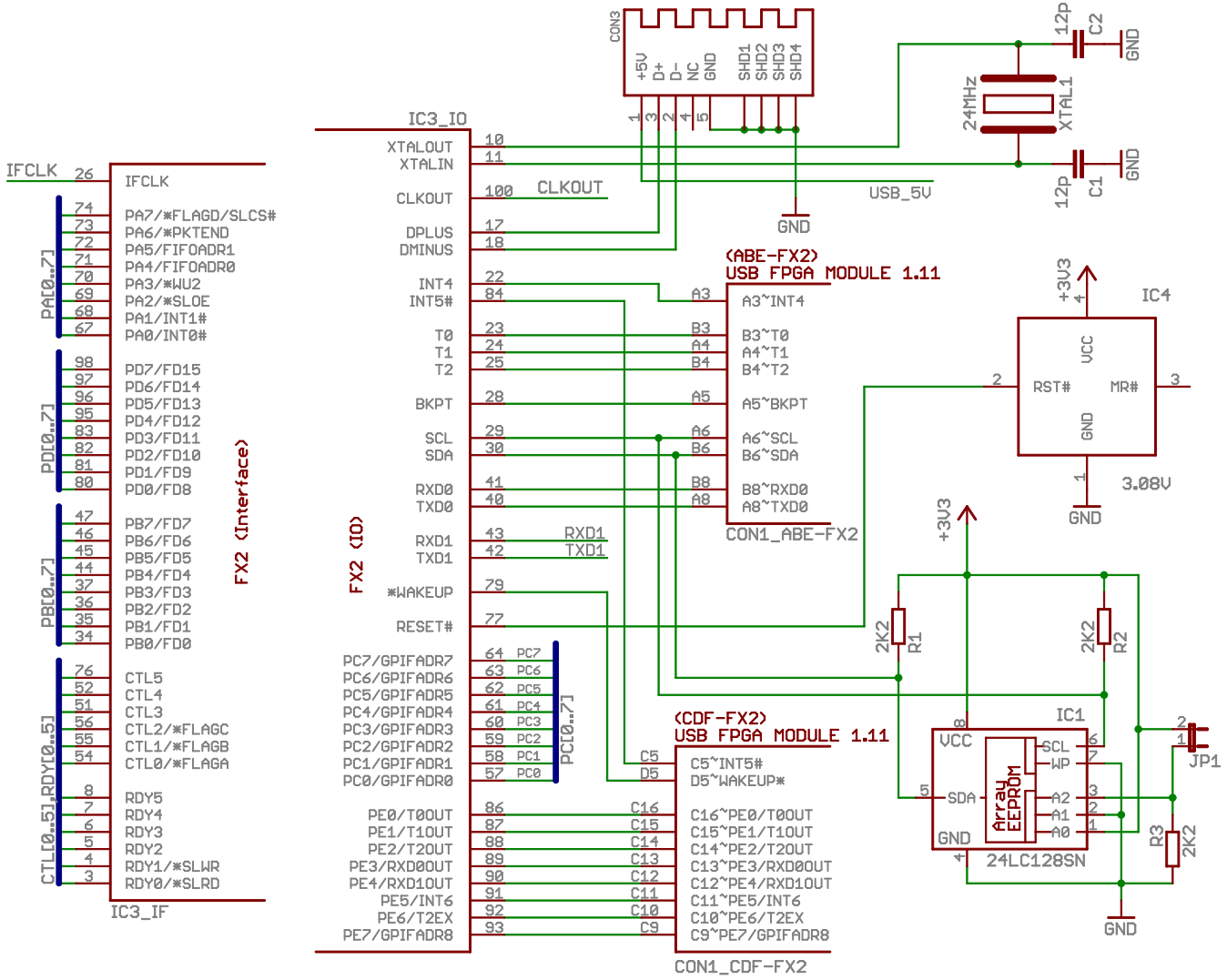
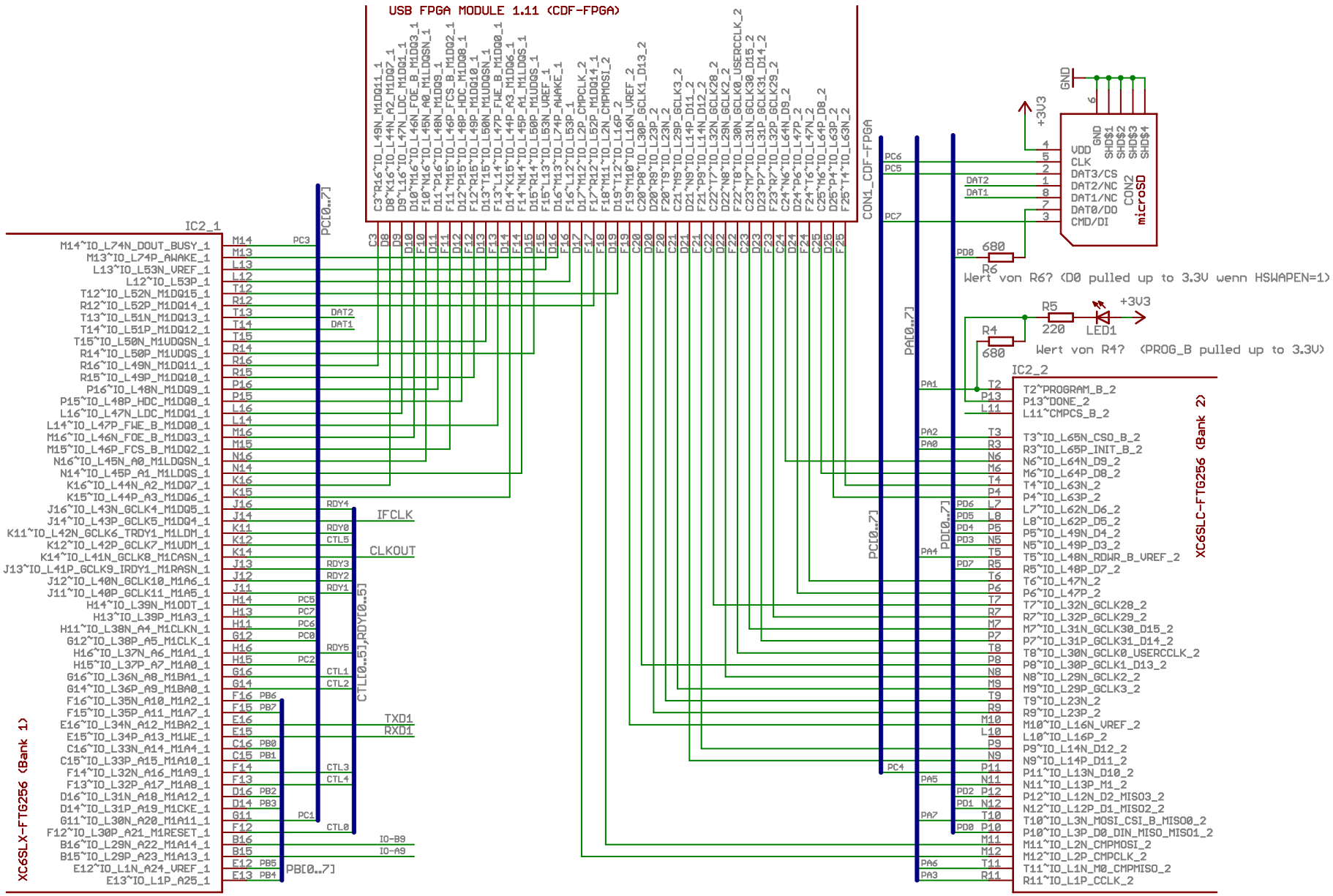
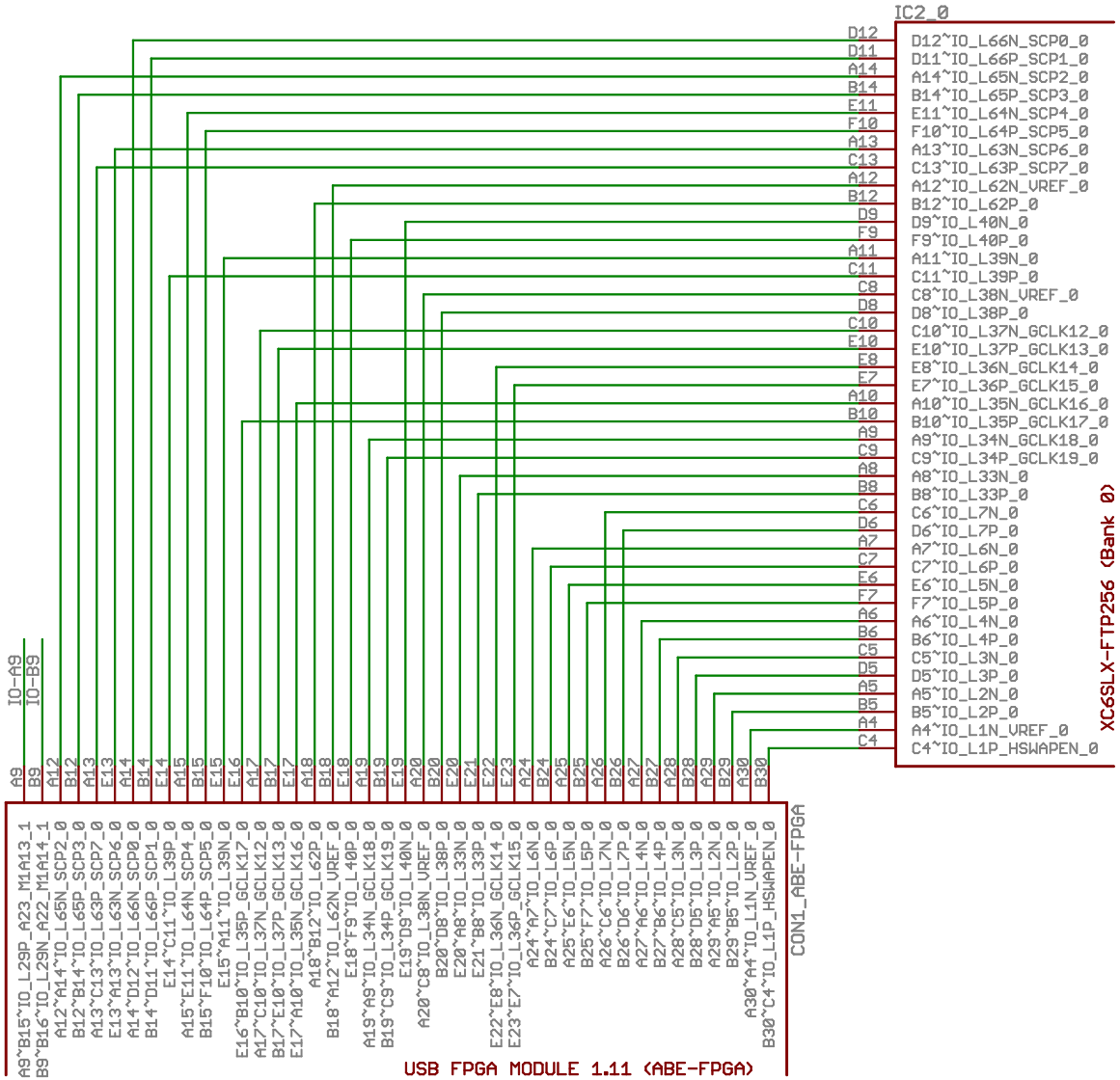
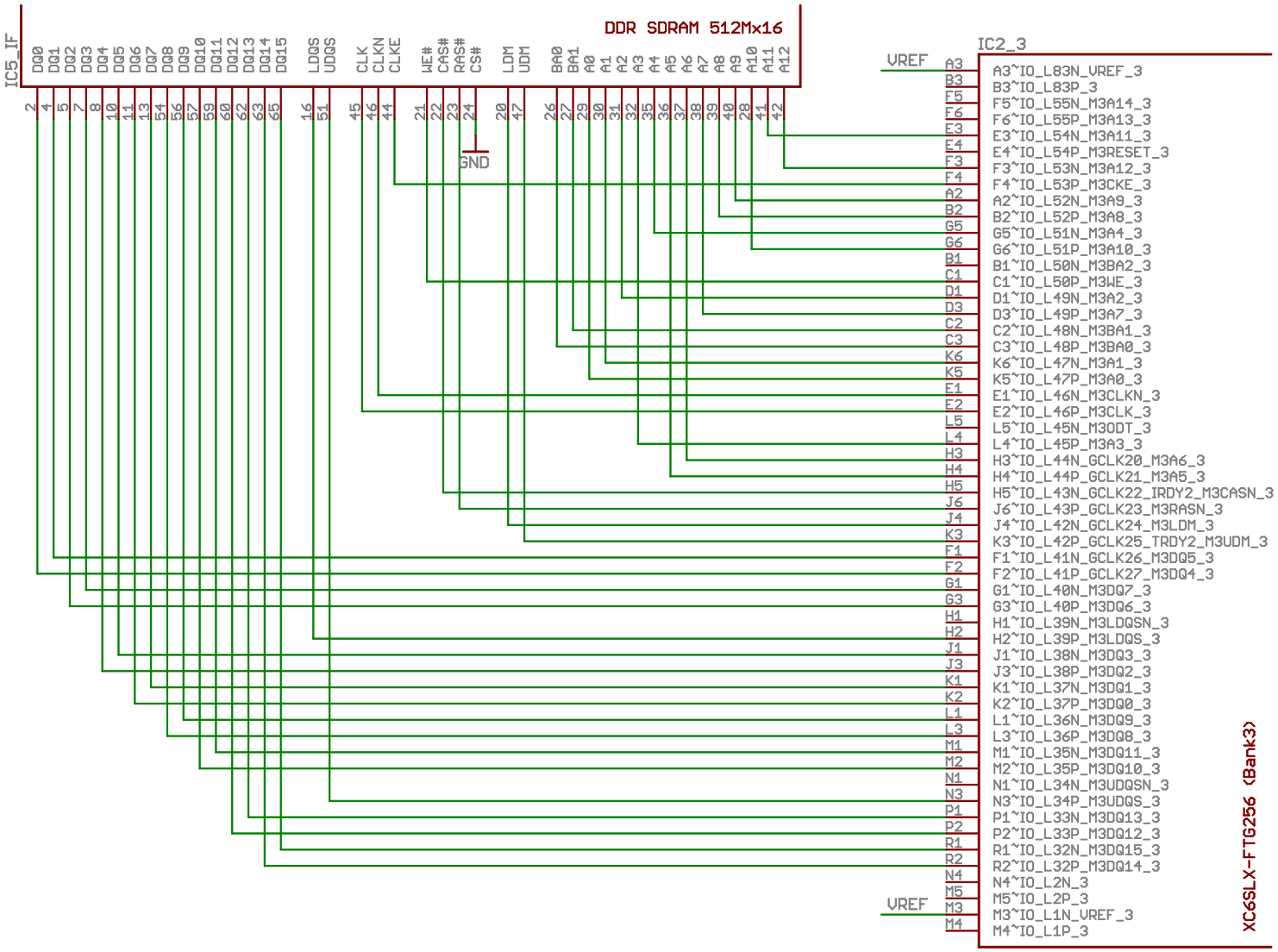
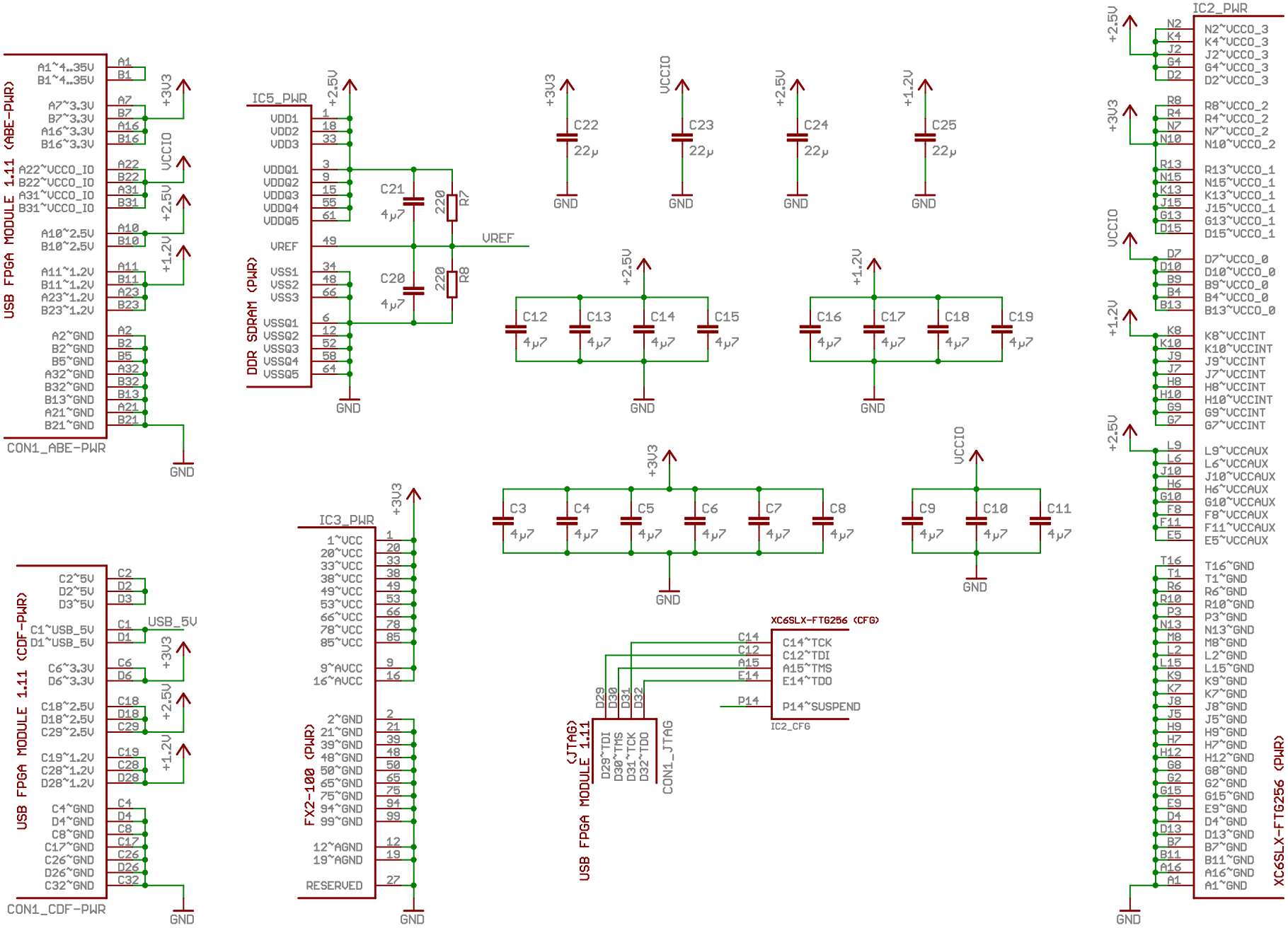

IFCLK
IC3_IF
FX2 (Interface)
PA[0..7]
PD[0..7]
PB[0..7]
CTL[0..5],RDY[0..5]
IFCLK
PA7/*FLAGD/SLCS#
PA6/*PKTEND
PA5/FIFOADR1
PA4/FIFOADR0
PA3/*WU2
PA2/*SLOE
PA1/INT1#
PA0/INT0#
PD7/FD15
PD6/FD14
PD5/FD13
PD4/FD12
PD3/FD11
PD2/FD10
PD1/FD9
PD0/FD8
PB7/FD7
PB6/FD6
PB5/FD5
PB4/FD4
PB3/FD3
PB2/FD2
PB1/FD1
PB0/FD0
CTL5
CTL4
CTL3
CTL2/*FLAGC
CTL1/*FLAGB
CTL0/*FLAGA
RDY5
RDY4
RDY3
RDY2
RDY1/*SLWR
RDY0/*SLRD
IC3_IO
FX2 (IO)
XTALOUT
XTALIN
CLKOUT
DPLUS
DMINUS
INT4
INT5#
T0
T1
T2
BKPT
SCL
SDA
RXD0
TXD0
RXD1
TXD1
*WAKEUP
RESET#
PC7/GPIFADR7
PC6/GPIFADR6
PC5/GPIFADR5
PC4/GPIFADR4
PC3/GPIFADR3
PC2/GPIFADR2
PC1/GPIFADR1
PC0/GPIFADR0
PC[0..7]
PE0/T0OUT
PE1/T1OUT
PE2/T2OUT
PE3/RXD0OUT
PE4/RXD1OUT
PE5/INT6
PE6/T2EX
PE7/GPIFADR8
CLKOUT
RXD1
TXD1
CON3
+5V
D+
D-
NC
GND
SHD1
SHD2
SHD3
SHD4
USB_5V
GND
(ABE-FX2)
USB FPGA MODULE 1.11
A3~INT4
B3~T0
A4~T1
B4~T2
A5~BKPT
A6~SCL
B6~SDA
B8~RXD0
A8~TXD0
CON1_ABE-FX2
(CDF-FX2)
USB FPGA MODULE 1.11
C5~INT5#
D5~WAKEUP*
C16~PE0/T0OUT
C15~PE1/T1OUT
C14~PE2/T2OUT
C13~PE3/RXD0OUT
C12~PE4/RXD1OUT
C11~PE5/INT6
C10~PE6/T2EX
C9~PE7/GPIFADR8
CON1_CDF-FX2
24MHz
XTAL1
12p
C2
C1
GND
+3V3
IC4
VCC
RST#
MR#
GND
3.08V
2K2
R1
R2
R3
IC1
VCC
SCL
WP
SDA
A2
A1
A0
GND
Array EEPROM
24LC128SN
JP1


USB FPGA MODULE 1.11 (CDF-FPGA)
CON1_CDF-FPGA
IC2_1
XC6SLX-FTG256 (Bank 1)
IC2_2
XC6SLC-FTG256 (Bank 2)
CON2
microSD
VDD
CLK
DAT3/CS
DAT2/NC
DAT1/NC
DAT0/DO
CMD/DI
GND
SHD$1
SHD$2
SHD$3
SHD$4
+3V3
R6
680
Wert von R6? (D0 pulled up to 3.3V wenn HSWAPEN=1)
R5
220
LED1
R4
680
Wert von R4? (PROG_B pulled up to 3.3V)
PC[0..7]
PA[0..7]
PD[0..7]
PB[0..7]
CTL[0..5],RDY[0..5]
IFCLK
CLKOUT
TXD1
RXD1
IO-B9
IO-A9
T2~PROGRAM_B_2
P13~DONE_2
L11~CMPCS_B_2
T3~IO_L65N_CSO_B_2
R3~IO_L65P_INIT_B_2
N6~IO_L64N_D9_2
M6~IO_L64P_D8_2
T4~IO_L63N_2
P4~IO_L63P_2
L7~IO_L62N_D6_2
L8~IO_L62P_D5_2
P5~IO_L49N_D4_2
N5~IO_L49P_D3_2
T5~IO_L48N_RDWR_B_VREF_2
R5~IO_L48P_D7_2
T6~IO_L47N_2
P6~IO_L47P_2
T7~IO_L32N_GCLK28_2
R7~IO_L32P_GCLK29_2
M7~IO_L31N_GCLK30_D15_2
P7~IO_L31P_GCLK31_D14_2
T8~IO_L30N_GCLK0_USERCCLK_2
P8~IO_L30P_GCLK1_D13_2
N8~IO_L29N_GCLK2_2
M9~IO_L29P_GCLK3_2
T9~IO_L23N_2
R9~IO_L23P_2
M10~IO_L16N_VREF_2
L10~IO_L16P_2
P9~IO_L14N_D12_2
N9~IO_L14P_D11_2
P11~IO_L13N_D10_2
N11~IO_L13P_M1_2
P12~IO_L12N_D2_MISO3_2
N12~IO_L12P_D1_MISO2_2
T10~IO_L3N_MOSI_CSI_B_MISO0_2
P10~IO_L3P_D0_DIN_MISO_MISO1_2
M11~IO_L2N_CMPMOSI_2
M12~IO_L2P_CMPCLK_2
T11~IO_L1N_M0_CMPMISO_2
R11~IO_L1P_CCLK_2


IC2_0
XC6SLX-FTP256 (Bank 0)
D12 D12~IO_L66N_SCP0_0
D11 D11~IO_L66P_SCP1_0
A14 A14~IO_L65N_SCP2_0
B14 B14~IO_L65P_SCP3_0
E11 E11~IO_L64N_SCP4_0
F10 F10~IO_L64P_SCP5_0
A13 A13~IO_L63N_SCP6_0
C13 C13~IO_L63P_SCP7_0
A12 A12~IO_L62N_VREF_0
B12 B12~IO_L62P_0
D9 D9~IO_L40N_0
F9 F9~IO_L40P_0
A11 A11~IO_L39N_0
C11 C11~IO_L39P_0
C8 C8~IO_L38N_VREF_0
D8 D8~IO_L38P_0
C10 C10~IO_L37N_GCLK12_0
E10 E10~IO_L37P_GCLK13_0
E8 E8~IO_L36N_GCLK14_0
E7 E7~IO_L36P_GCLK15_0
A10 A10~IO_L35N_GCLK16_0
B10 B10~IO_L35P_GCLK17_0
A9 A9~IO_L34N_GCLK18_0
C9 C9~IO_L34P_GCLK19_0
A8 A8~IO_L33N_0
B8 B8~IO_L33P_0
C6 C6~IO_L7N_0
D6 D6~IO_L7P_0
A7 A7~IO_L6N_0
C7 C7~IO_L6P_0
E6 E6~IO_L5N_0
F7 F7~IO_L5P_0
A6 A6~IO_L4N_0
B6 B6~IO_L4P_0
C5 C5~IO_L3N_0
D5 D5~IO_L3P_0
A5 A5~IO_L2N_0
B5 B5~IO_L2P_0
A4 A4~IO_L1N_VREF_0
C4 C4~IO_L1P_HSWAPEN_0
IO-A9
IO-B9
A9 A9~B15~IO_L29P_A23_M1A13_1
B9 B9~B16~IO_L29N_A22_M1A14_1
A12 A12~A14~IO_L65N_SCP2_0
B12 B12~B14~IO_L65P_SCP3_0
A13 A13~C13~IO_L63P_SCP7_0
E13 E13~A13~IO_L63N_SCP6_0
A14 A14~D12~IO_L66N_SCP0_0
B14 B14~D11~IO_L66P_SCP1_0
E14 E14~C11~IO_L39P_0
A15 A15~E11~IO_L64N_SCP4_0
B15 B15~F10~IO_L64P_SCP5_0
E15 E15~A11~IO_L39N_0
E16 E16~B10~IO_L35P_GCLK17_0
A17 A17~C10~IO_L37N_GCLK12_0
B17 B17~E10~IO_L37P_GCLK13_0
E17 E17~A10~IO_L35N_GCLK16_0
A18 A18~B12~IO_L62P_0
B18 B18~A12~IO_L62N_VREF_0
E18 E18~F9~IO_L40P_0
A19 A19~A9~IO_L34N_GCLK18_0
B19 B19~C9~IO_L34P_GCLK19_0
E19 E19~D9~IO_L40N_0
A20 A20~C8~IO_L38N_VREF_0
B20 B20~D8~IO_L38P_0
E20 E20~A8~IO_L33N_0
E21 E21~B8~IO_L33P_0
E22 E22~E8~IO_L36N_GCLK14_0
E23 E23~E7~IO_L36P_GCLK15_0
A24 A24~A7~IO_L6N_0
B24 B24~C7~IO_L6P_0
A25 A25~E6~IO_L5N_0
B25 B25~F7~IO_L5P_0
A26 A26~C6~IO_L7N_0
B26 B26~D6~IO_L7P_0
A27 A27~A6~IO_L4N_0
B27 B27~B6~IO_L4P_0
A28 A28~C5~IO_L3N_0
B28 B28~D5~IO_L3P_0
A29 A29~A5~IO_L2N_0
B29 B29~B5~IO_L2P_0
A30 A30~A4~IO_L1N_VREF_0
B30 B30~C4~IO_L1P_HSWAPEN_0
CON1_ABE-FPGA
USB FPGA MODULE 1.11 (ABE-FPGA)


DDR SDRAM 512Mx16
IC5_IF
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
LDQS UDQS
CLK CLKN CLKE
WE# CAS# RAS# CS#
LDM UDM
BA0 BA1 A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12
2 4 5 7 8 10 11 13 54 56 57 59 60 62 63 65 16 51 45 46 44 21 22 23 24 20 47 26 27 29 30 31 32 35 36 37 38 39 40 28 41 42
GND
VREF
VREF
IC2_3
A3 B3 F5 F6 E3 E4 F3 F4 A2 B2 G5 G6 B1 C1 D1 D3 C2 C3 K6 K5 E1 E2 L5 L4 H3 H4 H5 J6 J4 K3 F1 F2 G1 G3 H1 H2 J1 J3 K1 K2 L1 L3 M1 M2 N1 N3 P1 P2 R1 R2 N4 M5 M3 M4
A3~IO_L83N_VREF_3
B3~IO_L83P_3
F5~IO_L55N_M3A14_3
F6~IO_L55P_M3A13_3
E3~IO_L54N_M3A11_3
E4~IO_L54P_M3RESET_3
F3~IO_L53N_M3A12_3
F4~IO_L53P_M3CKE_3
A2~IO_L52N_M3A9_3
B2~IO_L52P_M3A8_3
G5~IO_L51N_M3A4_3
G6~IO_L51P_M3A10_3
B1~IO_L50N_M3BA2_3
C1~IO_L50P_M3WE_3
D1~IO_L49N_M3A2_3
D3~IO_L49P_M3A7_3
C2~IO_L48N_M3BA1_3
C3~IO_L48P_M3BA0_3
K6~IO_L47N_M3A1_3
K5~IO_L47P_M3A0_3
E1~IO_L46N_M3CLKN_3
E2~IO_L46P_M3CLK_3
L5~IO_L45N_M3ODT_3
L4~IO_L45P_M3A3_3
H3~IO_L44N_GCLK20_M3A6_3
H4~IO_L44P_GCLK21_M3A5_3
H5~IO_L43N_GCLK22_IRDY2_M3CASN_3
J6~IO_L43P_GCLK23_M3RASN_3
J4~IO_L42N_GCLK24_M3LDM_3
K3~IO_L42P_GCLK25_TRDY2_M3UDM_3
F1~IO_L41N_GCLK26_M3DQ5_3
F2~IO_L41P_GCLK27_M3DQ4_3
G1~IO_L40N_M3DQ7_3
G3~IO_L40P_M3DQ6_3
H1~IO_L39N_M3LDQSN_3
H2~IO_L39P_M3LDQS_3
J1~IO_L38N_M3DQ3_3
J3~IO_L38P_M3DQ2_3
K1~IO_L37N_M3DQ1_3
K2~IO_L37P_M3DQ0_3
L1~IO_L36N_M3DQ9_3
L3~IO_L36P_M3DQ8_3
M1~IO_L35N_M3DQ11_3
M2~IO_L35P_M3DQ10_3
N1~IO_L34N_M3UDQSN_3
N3~IO_L34P_M3UDQS_3
P1~IO_L33N_M3DQ13_3
P2~IO_L33P_M3DQ12_3
R1~IO_L32N_M3DQ15_3
R2~IO_L32P_M3DQ14_3
N4~IO_L2N_3
M5~IO_L2P_3
M3~IO_L1N_VREF_3
M4~IO_L1P_3
XC6SLX-FTG256 (Bank3)


USB FPGA MODULE 1.11 (ABE-PWR)
CON1_ABE-PWR
A1~4..35V
B1~4..35V
A7~3.3V
B7~3.3V
A16~3.3V
B16~3.3V
A22~VCCO_IO
B22~VCCO_IO
A31~VCCO_IO
B31~VCCO_IO
A10~2.5V
B10~2.5V
A11~1.2V
B11~1.2V
A23~1.2V
B23~1.2V
A2~GND
B2~GND
B5~GND
A32~GND
B32~GND
B13~GND
A21~GND
B21~GND
+3V3
VCCIO
+2.5V
+1.2V
GND
IC5_PWR
DDR SDRAM (PWR)
VDD1
VDD2
VDD3
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VREF
VSS1
VSS2
VSS3
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
C21
4µ7
C20
4µ7
220
R7
R8
VREF
C22
22µ
C23
22µ
C24
22µ
C25
22µ
C12
C13
C14
C15
C16
C17
C18
C19
4µ7
C3
C4
C5
C6
C7
C8
C9
C10
C11
USB FPGA MODULE 1.11 (CDF-PWR)
CON1_CDF-PWR
C2~5V
D2~5V
D3~5V
C1~USB_5V
D1~USB_5V
USB_5V
C6~3.3V
D6~3.3V
C18~2.5V
D18~2.5V
C29~2.5V
C19~1.2V
C28~1.2V
D28~1.2V
C4~GND
D4~GND
C8~GND
C17~GND
C26~GND
D26~GND
C32~GND
IC3_PWR
FX2-100 (PWR)
1~VCC
20~VCC
33~VCC
38~VCC
49~VCC
53~VCC
66~VCC
78~VCC
85~VCC
9~AVCC
16~AVCC
2~GND
21~GND
39~GND
48~GND
50~GND
65~GND
75~GND
94~GND
99~GND
12~AGND
19~AGND
RESERVED
USB FPGA MODULE 1.11 (JTAG)
CON1_JTAG
D29~TDI
D30~TMS
D31~TCK
D32~TDO
XC6SLX-FTG256 (CFG)
IC2_CFG
C14~TCK
C12~TDI
A15~TMS
E14~TDO
P14~SUSPEND
IC2_PWR
XC6SLX-FTG256 (PWR)
N2~VCCO_3
K4~VCCO_3
J2~VCCO_3
G4~VCCO_3
D2~VCCO_3
R8~VCCO_2
R4~VCCO_2
N7~VCCO_2
N10~VCCO_2
R13~VCCO_1
N15~VCCO_1
K13~VCCO_1
J15~VCCO_1
G13~VCCO_1
D15~VCCO_1
D7~VCCO_0
D10~VCCO_0
B9~VCCO_0
B4~VCCO_0
B13~VCCO_0
K8~VCCINT
K10~VCCINT
J9~VCCINT
J7~VCCINT
H8~VCCINT
H10~VCCINT
G9~VCCINT
G7~VCCINT
L9~VCCAUX
L6~VCCAUX
J10~VCCAUX
H6~VCCAUX
G10~VCCAUX
F8~VCCAUX
F11~VCCAUX
E5~VCCAUX
T16~GND
T1~GND
R6~GND
R10~GND
P3~GND
N13~GND
M8~GND
L2~GND
L15~GND
K9~GND
K7~GND
J8~GND
J5~GND
H9~GND
H7~GND
H12~GND
G8~GND
G2~GND
G15~GND
E9~GND
D4~GND
D13~GND
B7~GND
B11~GND
A16~GND
A1~GND